Walchand College of Engineering, Sangli

(A Government Aided Autonomous Institute)

Course Contents (Syllabus) for

First and Second Year M. Tech. (Electronics Engineering) Sem ï I to IV

AY 2020-21

Walchand College of Engineering, Sangli
(An Autonomous Institute)
Teaching and Evaluation Scheme effective from 2020-21
First year M. Tech. Program in Electronics Engineering
Semester I

Course			Teaching Scheme				Evaluation Scheme		
Category	**Code**	**Name**	**L**	**T**	**P**	**Credits**	**Component**	**Marks**	
								Max	**Min for Passing**
PC	4IC501	Research Methodology	2	0	0	2	ISE 1	10	40
							MSE	30	
							ISE 2	10	
							ESE	50	20
PC	4EN501	Advanced Digital Signal Processing	3	0	0	3	ISE 1	10	40
							MSE	30	
							ISE 2	10	
							ESE	50	20
PC	4EN502	Embedded System Design	3	0	0	3	ISE 1	10	40
							MSE	30	
							ISE 2	10	
							ESE	50	20
PC	4EN551	Electronics Lab 1	0	0	4	2	ISE 1	25	40
							MSE	25	
							ISE 2	25	
							ESE	25	
PE	Refer List	Professional Elective 1	3	0	0	3	ISE 1	10	40
							MSE	30	
							ISE 2	10	
							ESE	50	20
PE	Refer List	Professional Elective 2	3	0	0	3	ISE 1	10	40
							MSE	30	
							ISE 2	10	
							ESE	50	20
PE	4EN552	Electronics Lab 2	0	0	4	2	ISE 1	25	40
							MSE	25	
							ISE 2	25	
							ESE	25	
MC	Refer List	Mandatory Life Skill Course	2	0	0	0	ISE 1	10	40
							MSE	30	
							ISE 2	10	
							ESE	50	20
VAPC, VALS		Refer List	0	0	0	0	-	-	-

Total	14	0	8	18	**Total Credits: 18** **Total Contact Hrs: 22**

Professional Elective 1		
Sr.No.	Course Code	Course name
1	4EN511	Digital VLSI Design
2	4EN512	Information Theory and Coding
Professional Elective 2		
Sr.No.	Course Code	Course name
1	4EN515	Biomedical Signal Processing
2	4EN516	Embedded Linux Programming

Walchand College of Engineering, Sangli
(An Autonomous Institute)
Teaching and Evaluation Scheme effective from 2018-19
First year M. Tech. Program in Electronics Engineering
Semester II

Course			Teaching Scheme				Evaluation Scheme		
Category	**Code**	**Name**	**L**	**T**	**P**	**Credits**	**Component**	**Marks**	
								Max	**Min for Passing**
PC	4EN521	Advanced Embedded Programming	3	0	0	3	ISE 1	10	40
							MSE	30	
							ISE 2	10	
							ESE	50	20
PC	4EN522	Advanced Communication Networks and IoT	3	0	0	3	ISE 1	10	40
							MSE	30	
							ISE 2	10	
							ESE	50	20
PC	4EN571	Electronics Lab 3	0	0	4	2	ISE 1	25	40
							MSE	25	
							ISE 2	25	
							ESE	25	
PC	4EN572	Industrial Project	0	0	4	2	ISE 1	25	40
							MSE	25	
							ISE 2	25	
							ESE	25	
PE	Refer List	Professional Elective 3	3	0	0	3	ISE 1	10	40
							MSE	30	
							ISE 2	10	
							ESE	50	20
PE	Refer List	Professional Elective 4	3	0	0	3	ISE 1	10	40
							MSE	30	
							ISE 2	10	
							ESE	50	20
PC	4EN573	Electronics Lab 4	0	0	4	2	ISE 1	25	40
							MSE	25	
							ISE 2	25	
							ESE	25	
MC	Refer List	Mandatory Life Skill Course	2	0	0	0	ISE 1	10	40
							MSE	30	
							ISE 2	10	
							ESE	50	20
VAPC									

VALS								
Total			14	0	12	18	**Total Credits: 18** **Total Contact Hrs: 26**	

Professional Elective 3		
Sr.No.	Course Code	Course Name
1	4EN531	RTL Simulation and Synthesis with PLDs
2	4EN532	Pattern Recognition and Image Analysis
Professional Elective 4		
1	4EN535	Wireless Sensor Networks

Value Added Life Skill Courses		

Walchand College of Engineering, Sangli

(An Autonomous Institute)

Teaching and Evaluation Scheme effective from 2019-20

Second year M. Tech. Program in Electronics Engineering

Semester III

Course			Teaching Scheme				Evaluation Scheme		
Category	**Code**	**Name**	**L**	**T**	**P**	**Credits**	**Component**	**Marks**	
								Max	**Min for Passing**
PC	3EN690	Dissertation phase I	0	0	8	4	ISE 1	25	40
							MSE	25	
							ISE 2	25	
							ESE	25	
PC	3EN691	Dissertation phase II	0	0	4	2	ISE 1	25	40
							MSE	25	
							ISE 2	25	
							ESE	25	
PC	3EN692	Dissertation phase II	0	0	8	4	ISE 1	25	40
							MSE	25	
							ISE 2	25	
							ESE	25	
PE	Refer List	Professional Elective V	3	0	0	3	ISE 1	10	40
							MSE	30	
							ISE 2	10	
							ESE	50	20
MC	3IC6**	Mandatory Non Credit Course	2	0	0	0	ISE 1	35	40
							MSE	30	
							ISE 2	35	
							ESE	0	
Total			5	0	20	13	**Total Credits: 13** **Total Contact Hrs: 25**		

Professional Elective Course V		
Sr.No.	Course Code	Course Name
1	3EN611	Artificial Intelligence
2	3EN612	Advanced Automotive Electronics
3	3EN613	Introduction to Machine Learning
4	3EN614	DSP Architectures

List of Mandatory Non Credit Course		
Sr.No.	Course Code	Course Name
1	3IC601	Constitution of India
2	3IC602	Pedagogy of Studies
3	3IC603	Disaster Management
4	3IC604	Value Education

Walchand College of Engineering, Sangli

(An Autonomous Institute)

Teaching and Evaluation Scheme effective from 2019-20

Second year M. Tech. Program in Electronics Engineering

Semester IV									
Course			**Teaching Scheme**				**Evaluation Scheme**		
Category	**Code**	**Name**	**L**	**T**	**P**	**Credits**	**Component**	**Marks**	
								Max	**Min for Passing**
PC	3ST693	Dissertation phase III	0	0	8	4	ISE 1	25	40
							MSE	25	
							ISE 2	25	
							ESE	25	
PC	3ST694	Dissertation phase IV	0	0	8	4	ISE 1	25	40
							MSE	25	
							ISE 2	25	
							ESE	25	
PC	3ST695	Dissertation phase IV	0	0	16	8	ISE 1	25	40
							MSE	25	
							ISE 2	25	
							ESE	25	
MC	3IC6**	Mandatory Non Credit Course	2	0	0	0	ISE 1	35	40
							MSE	30	
							ISE 2	35	
							ESE	0	
Total			0	0	32	16	**Total Credits: 16** **Total Contact Hrs: 34**		

Semester	**I**	**II**	**III**	**IV**	**Total**
Credits	18	18	13	16	65

Semester I

Title of the Course and Course Code:	L	T	P	Cr
Research Methodology for Electronics Engineers 4IC501	2	0	0	2

Pre-Requisite Courses: Electronics Engineering

Textbooks:

1. C. R. Kothari, Research Methodology Methods and Techniques, New Age international, 2nd Edition, 2009
2. Deepak Chopra and Neena Sondhi, *Research Methodology : Concepts and cases,* Vikas Publishing House, New Delhi, 2008

References:

1. E. Philip and Derek Pugh, How to get a Ph. D. – a handbook for students and their supervisors, Open university press,5th Edition,2010
2. Stuart Melville and Wayne Goddard, Research Methodology: An Introduction for Science & Engineering Students, Kenwyn, South Africa : Juta & Co. Ltd., 1996.

Course Objectives :

1. To develop a research orientation among the students and to acquaint them with fundamentals of research methods
2. To develop understanding of the basic framework of research process and techniques.
3. To identify various sources of information for literature review and data collection.
4. To develop an understanding of the ethical dimensions of conducting applied research.
5. Appreciate the components of scholarly writing.

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive Level	Descriptor
CO1	Identify/formulate research the problem for M. Tech. dissertation	Remembering	Describe
CO2	Articulate a review paper in the format of standard Journal/transactions by reviewing at least 10 papers (from standard Journals /transactions /Reference Books/Handbooks etc) related to a	Understanding	Explain
CO3	To deliver a seminar on the same, prepare a presentation giving critical analysis of the subject and possible outcomes	Evaluating	Discuss
CO4	Write dissertation/thesis after completion of the work for the degrees of M. Tech.	Creating	Compose

CO-PO Mapping :

PO	1	2	3	4	5	6
CO1	**2**					
CO2		**2**				
CO3		**2**				
CO4				1		
3-H, 2-M, 1-L						

Assessment:

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weightage respectively.

Assessment	Marks
ISE 1	10
MSE	30
ISE 2	10
ESE	50

ISE 1 and ISE 2 are based on assignment, oral, seminar, test (surprise/declared/quiz), and group discussion.[One assessment tool per ISE. The assessment tool used for ISE 1 shall not be used for ISE 2]

MSE: Assessment is based on 50% of course content (Normally first three modules)

ESE: Assessment is based on 100% course content with70-80% weightage for course content (normally last three modules) covered after MSE.

Course Contents:

Module 1	**Hr**
Introduction Concepts of Research, Meaning and Objectives of Research, Research Process, Types of Research, Criteria of Good Research, Research Problem – Identifying and Defining, Research Proposals – Types, contents, Sponsoring agency's requirements, Ethical aspects, IPR issues like patenting, copyrights	**4**
Module 2	**Hr**
Research Design Meaning, Need and Types of research design, Literature Survey and Review, Research Design Process, Measurement and scaling techniques, Data Collection – concept, types and methods, Processing and analysis of data, Quantitative Techniques Sampling fundamentals, Design of Experiments.	**4**
Module 3	**Hr**
Quantitative Techniques Sampling fundamentals, Testing of hypothesis using various tests like Multivariate analysis, Use of standard statistical software, Data processing, Preliminary data analysis and interpretation, Uni-variate and bi-variate analysis of data, testing of hypotheses, techniques such as ANOVA, Chi square test etc., Nonparametric tests. Correlation and regression analysis	**5**
Module 4	**Hr**
Measurements based research methods in Signal and Image Processing, Graphics, Vision and Pattern Recognition, , Induction Vs Deduction, Deductive and Inductive Methods in Signal and Image Processing, Graphics, Vision and Pattern, Recognition; Hypothetical-Deductive Method, Repetitions, Patterns, Identity, Causality And Determinism, Godel's Theorem, Fuzzy Logic, Research in the area of VLSI	**5**
Module 5	**Hr**
Research Communication, Writing a conference paper, Journal Paper, Technical report, dissertation/thesis writing. Presentation techniques, Patents and other IPRs, software used for report writing such as WORD, Latex etc.	**5**
Module 6	**Hr**
Case studies: Related to Electronics Engineering.	**3**

Module wise Measurable Students Learning Outcomes :

Module 1: Describe a range of quantitative and qualitative research designs

Module 2: Identify the advantages and disadvantages associated with research designs

Module 3: Explain the testing of hypothesis

Module 4: Recognize the keys in Electronics Engineering research

Module 5: Write and present review paper in conference or in journal

Module 6: Design an appropriate mixed-method research study to solve a problem in the field of Electronics Engineering

Title of the Course and Course Code: Advanced Digital Signal Processing 4EN501	L	T	P	Cr
	3	0	0	3

Pre-Requisite Courses: Signals and Systems, Digital Signal Processing

Textbooks:

1. Sanjit K. Mitra, "Digital Signal Processing – A Computer based approach", Tata McGraw-Hill, 4th Edition , 2013
2. Bernard Widrow, Samuel D. Stearns "Adaptive Signal Processing,", Prentice-Hall, Englewood Cli, NJ, 1985

References:

1. J. G. Proakis, Dimitris K Manolakis, "Advanced Digital Signal Processing Principals, Algorithms and Applications,", Pearson,2007

Course Objectives :

1. To illustrate the concepts of Advanced Signal Processing.
2. To explain the different techniques for design of filters and multirate systems.
3. To enable the students for the design and development of Adaptive DSP systems.

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive	
		Level	**Descriptor**
CO1	Explain the basic and advanced signal processing concepts.	Understanding	Discuss
CO2	Design FIR and IIR filters with given specifications.	Creating, Applying	Design, Solve
CO3	Analyse the various algorithms related with multi-rate DSP	Analysing	Explain
CO4	Illustrate adaptive signal processing algorithms	Applying	Demonstrate

CO-PO Mapping :

PO	1	2	3	4	5	6
CO1			2			
CO2						1
CO3				2		
CO4			1			
3-H, 2-M, 1-L						

Assessment:

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weightage respectively.

Assessment	Marks
ISE 1	10
MSE	30
ISE 2	10
ESE	50

ISE 1 and ISE 2 are based on assignment, oral, seminar, test (surprise/declared/quiz), and group discussion.[One assessment tool per ISE. The assessment tool used for ISE 1 shall not be used for ISE 2]

MSE: Assessment is based on 50% of course content (Normally first three modules)
ESE: Assessment is based on 100% course content with70-80% weightage for course content (normally last three modules) covered after MSE.

Course Contents:

1	**Module 1: Review of Digital Signal Processing**	**Hrs**
	Discrete Time Signals and systems, LTI Systems, Basic Signal Processing Operations, Discrete Time Systems-Classification, impulse and step responses, phase and group delays. Time domain and frequency domain characterization of LTI discrete time systems, Z Transform, Transfer function	**8**
2	**Module 2: DSP Structures**	**Hrs**
	Block Diagram Representation, Equivalent Structures, Basic FIR Digital Filter Structures, Basic IIR Digital Filter Structures, All pass Filters, Tuneable IIR Digital Filters, IIR Tapped Cascaded Lattice Structures, FIR Cascaded Lattice Structures, Parallel All pass Realization of IIR Transfer Functions	**6**
3	**Module 3: DFT Computation Techniques**	**Hrs**
	DFT-Definition and properties, symmetry properties, Circular convolution, Computation of DFT, Decimation in time (DIT) and Decimation in Frequency (DIF) Fast Fourier transform (FFT) algorithms , Linear filtering using FFT- overlap add, overlap save methods, Goertzel Algorithm	**6**
4	**Module 4: Filter Design Techniques**	**Hrs**
	Bilinear Transformation Method of IIR Filter Design, Design of Low pass IIR Digital Filters, Design of High pass, Band pass and Band stop IIR Digital Filters, Spectral Transformations of IIR Filters, FIR Filter Design Based on Windowed series, Design of Digital Filters with Least-Mean-Square Error, Constrained Least-Square Design of FIR Digital Filters	**8**
5	**Module5: Multi-rate Signal Processing**	**Hrs**
	The Basic Sample Rate Alteration Devices, Filters in Sampling Rate Alteration Systems, Multistage Design of Decimator and Interpolator, The Poly phase Decomposition, Arbitrary-Rate Sampling Rate Converter, Digital Filters Banks, Two-Channel Quadrature-Mirror Filter bank	**6**
6	**Module 6: Introduction to adaptive signal processing**	**Hrs**
	Introduction to Adaptive Filters, Steepest descent technique, LMS algorithm-Convergence analysis, Learning curve, SVD.	**6**

Module wise Measurable Students Learning Outcomes :

Module 1: Discuss the Digital Signal Processing concepts
Module 2 : Explain and construct the DSP structures
Module 3 : Solve the problems using DFT algorithms
Module 4 : Design FIR and IIR filter
Module 5 : Explain multi rate signal processing
Module 6 : Demonstrate adaptive signal processing algorithms

Tutorial: Tutorial will be engaged in either of following

1. Solving numerical
2. Writing and executing MATLAB programs for various algorithms in ADSP

Title of the Course and Course Code:	L	T	P	Cr
Embedded System Design 4EN502	3	0	0	3

Pre-Requisite Courses: Microprocessors / Microcontrollers

Textbooks:

1. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2nd Edition
2. Frank Vahid and Tony Givargis, "Embedded System Design", Wiley

References:

1. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing", Morgan Kaufman Publication
2. Steve furber, "ARM System-on-Chip Architecture", Pearson Education
3. Frank Vahid and Tony Givargis, "Embedded System Design", Wiley
4. Technical references and user manuals on www.arm.com, NXP Semiconductor www.nxp.com and Texas Instruments www.ti.com, ST Microelectronics www.st.com.

Course Objectives : At the end of this course, students will be able to

1. Understand ARM processor core architecture with several features of peripherals available on various embedded Cortex- M processors.
2. Understand interrupts and its programming with peripherals
3. Develop small embedded system by using the ARM processor core based systems and application software for it.
4. Use EDA tools to design embedded system PCB.
5. Interface various memories with cortex M processor.

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive Level	Descript
CO1	Illustrate Cortex M processor architecture and its features	Understanding	Illustrate
CO2	Develop programs for peripherals and interrupts	Applying	Develop
CO3	Designing embedded system hardware	Creating	Design
CO4	Design embedded system software.	Creating	Design
CO5	Design Interface for various memories with Embedded system	Creating	Design

CO-PO Mapping :

PO	1	2	3	4	5	6
CO1			2			
CO2				2		
CO3			2			
CO4				1		
3-H, 2-M, 1-L						

Assessment:

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weightage respectively.

Assessment	Marks
ISE 1	10
MSE	30
ISE 2	10
ESE	50

ISE 1 and ISE 2 are based on assignment, oral, seminar, test (surprise/declared/quiz), and group discussion.[One assessment tool per ISE. The assessment tool used for ISE 1 shall not be used for ISE 2]
MSE: Assessment is based on 50% of course content (Normally first three modules)
ESE: Assessment is based on 100% course content with70-80% weightage for course content (normally last three modules) covered after MSE.

Course Contents:

Module 1: ARM Cortex –M Architecture and Programming:	**6**
ARM Cortex M3/M4 Architecture, Registers, CPU status, Clock generation, Memory organization, Instruction Set, Programming model – Registers, Operation Modes, Embedded C Programming	
Module 2: Cortex M CPU Interrupts	**6**
Nested Vectored Interrupt Controller (NVIC), Vector table, Interrupt priorities, Interrupt Inputs and Pending behavior, Fault Exceptions, Supervisor and Pendable Service Call, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency, Startup files, initialization of peripherals interrupts, Interrupt routines programming.	
Module 3 : ARM Peripherals and Programming	**8**
On chip peripherals, GPIO, RTC, Watchdog, UART, I2C, I2S, ADC and SPI interfacing and Programming, Repetitive interrupt timer, PWM Block programming, CAN BUS programming, LIN bus programming, DMA programming,Writing LCD drives, Drivers for serial port communication	
Module 4: Embedded System Design and Testing	**8**
Design embedded system using Cortex-M3/M4 processors with SPI, UART, ADC, DAC, Memory, PWM peripherals. Hardware design issues, State Machine based Embedded Programming, Writing initialisation programs, Debugging techniques, Debugging with JTAG, Debugging with UART port.	
Module 5 : Memory	**6**
Types of Memory, static, dynamic, SDRAM, DDR RAM, Flash Memory chips, SD Card, Quad SPI Flash Interface with CPU.	
Module 6 : Hardware design issues	**6**
Selection of electronics components, Reading Schematic, Datasheets, footprints of various components, EDA tool for PCB design, Hierarchical design, Schematic and board layout design,	

board assembly process, board bring-up, cold and hot testing	

Module wise Measurable Students Learning Outcomes : student will able to

Module 1: Illustrate Cortex-M embedded CPU programming model

Module 2: Illustrate Cortex-M CPU interrupts and develop programs using interrupts

Module 3: Develop peripheral programming

Module 4: Design embedded system with peripherals

Module 5: Design embedded system with various memories

Module 6: Design schematic, PCB layout with EDA Tools and test it.

Title of the Course and Course Code:	**L**	**T**	**P**	**Cr**
Electronics Lab 1 4EN551	0	0	4	2

Pre-Requisite Courses: Microprocessors / Microcontrollers

Textbooks:

1. Joseph Yiu, “The definitive guide to ARM Cortex-M3”, Elsevier, 2nd Edition
2. Frank Vahid and Tony Givargis, “Embedded System Design”, Wiley
3. User and reference guide of LPC1768
4. Philips- An Indroduction to SDRAM and memory controller by Benny Akesson
5. Rigid Flex PCB design – by Ben Jordan

References:

1. Sloss Andrew N, Symes Dominic, Wright Chris, “ARM System Developer's Guide: Designing and Optimizing”, Morgan Kaufman Publication
2. Steve furber, “ARM System-on-Chip Architecture”, Pearson Education
3. Technical references and user manuals on www.arm.com, NXP Semiconductor www.nxp.com and Texas Instruments www.ti.com, ST Microelectronics www.st.com.

4. www.altium.com

Course Objectives : At the end of this course, students will be able to

1. Understand ARM processor core architecture with several features of peripherals available on LPC1768 embedded Cortex- M processors.
2. Understand interrupts and its programming with peripherals
3. Develop small embedded system by using the ARM processor core based systems and application software for it.
4. Use EDA tools to design embedded system PCB.
5. Interface various memories with cortex M processor.

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive Level	Descript
CO1	Illustrate Cortex M processor architecture and its features	Understanding	Illustrate
CO2	Develop and execute programs for peripherals and interrupts	Applying	Develop
CO3	Design and execute embedded system software	Creating	Design
CO4	Design embedded system PCB	Creating	Design

CO-PO Mapping :

PO	1	2	3	4	5	6
CO1			2			
CO2				2		
CO3			2			
CO4				1		
3-H, 2-M, 1-L						

Lab Assessment:

There are four components of lab assessment, LA1, LA2, LA3 and Lab ESE.
IMP: Lab ESE is a separate head of passing.

Assessment	Based on	Conducted by	Conduction and Marks Submission	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 4 Submission at the end of Week 5	25
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 5 to Week 8 Submission at the end of Week 9	25
LA3	Lab activities, attendance, journal	Lab Course Faculty	During Week 10 to Week 14 Submission at the end of Week 14	25
Lab ESE	Lab Performance and related documentation	Lab Course faculty	During Week 15 to Week 18 Submission at the end of Week 18	25

Week 1 indicates starting week of Semester.
Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments.

Course Contents:

1. Write Simple C Program with header files for array manipulations
2. Write C programs for GPIO and debug programs, see variables and waveforms.
3. Writing programs for UART in polling mode
4. Writing programs for SPI in interrupt mode
5. Writing programs for I2C and ADC etc. in polling mode
6. Writing programs for Interrupt vector table and writing interrupt programs for UART peripherals.
7. Write Programs with CMSIS for UART, SPI etc.
8. Design Embedded system using various peripherals in group of 2 students
9. Design PCB schematic for embedded system using LPC1768
10. Design Layout for schematic generated in Exp. 9

Experiment wise Measurable Students Learning Outcomes : student will able to

Experiment 1: Develop and execute Cortex-M embedded CPU programs for arrays
Experiment 2: Develop and execute Cortex-M CPU GPIO and debug it.
Experiment 3: Develop and execute peripheral UART programming in polling mode
Experiment 4: Develop and execute program for SPI in interrupt mode
Experiment 5: Develop and execute program for I2C and ADC in polling mode
Experiment 6: Develop and execute program for UART peripherals using interrupt
Experiment 7: Develop and execute program with CMSIS for UART, SPI etc
Experiment 8: Develop and execute program for Embedded system using various peripherals
Experiment 9: Design schematic with EDA Tools and test it.
Experiment 10: Design PCB layout with EDA Tools and test it.

Experiments using MATLAB :

1. Generation and analysis of different signals in time and frequency domains.
2. Study and applications of different transforms
3. Design of Digital Filter: IIR, FIR.
4. Design of multi rate signal system

Experiments using DSK 6713 DSP Kit

5. Introduction to DSK 6713 kit and CCS environment
6. Study of input/output, architecture of C6x processor
7. Digital filter design using DSK 6713
8. Implementation of DSP applications using DSK 6713

Title of the Course and Course Code: **Professional Elective I: Digital VLSI Design 4EN511**	**L**	**T**	**P**	**Cr**
	3	0	0	3

Pre-Requisite Courses: Digital Techniques

Textbooks:

1. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "*Digital Integrated Circuits, A System Perspective*", Pearson Education, Second Edition, First Indian Reprint, 2003.
2. Neil Weste, Kamran Eshraghian "*Principles of CMOS VLSI Design*", Addison Wesley/Pearson Education, 2010

References:

1. Kamran Eshraghian, Pucknell and Eshraghian "*Essentials of VLSI Circuits and Systems*", , Prentice-Hall (India), 2008
2. Sung-Mo Kang, Yusuf Leblebici "*CMOS Digital Integrated Circuits: Analysis and Design*", McGraw Hill Education (India), Third Edition, 2003
3. Neil Weste, David Harris, Ayan Banerjee "*CMOS VLSI Design*", Pearson Education, 2008

Course Objectives:

1. To explain the relevance of CMOS technology in implementing digital circuits.
2. To discuss in details various logic styles (static, dynamic) in implementing CMOS circuits and the effect of choosing a particular style on device performance from delay, power and area point of view.
3. To develop the architectures of few data-path designs (system building blocks) and an insight into extracting the functionality of displayed CMOS circuit.
4. To motivate the students to develop lifelong/self-learning attitude.

Course Learning Outcomes:

CO1: Apply the analytical expressions involving physical parameters, process parameters and electrical parameters to characterize the MOS transistors **by taking into account** the fundamental principles involved with MOS devices.

CO2: Analyze static and dynamic CMOS circuits logically to deduct the functionality of the circuits.

CO3: Analyze static and dynamic CMOS circuits numerically to compute the various device parameters and circuit performance parameters.

CO4: Select an appropriate logic style to design submicron MOS transistor based circuits using logical, analytical and computational skills

CO5: **Design** the self timed CMOS circuits, and synchronous circuits with built-in arbiters, synchronizers

CO6: Design with Justification the architectures/schematics of data path design viz adders, multipliers and data shifters.

CO-PO Mapping :

PO	1	2	3	4	5	6
CO1				2		
CO2						1
CO3						1
CO4			2			
CO5			1			
CO6						2
3-H, 2-M, 1-L						

Assessment:

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weightage respectively.

Assessment	Marks
ISE 1	10
MSE	30
ISE 2	10
ESE	50

ISE 1 and ISE 2 are based on assignment, oral, seminar, test (surprise/declared/quiz), and group discussion.[One assessment tool per ISE. The assessment tool used for ISE 1 shall not be used for ISE 2]
MSE: Assessment is based on 50% of course content (Normally first three modules)

ESE: Assessment is based on 100% course content with70-80% weightage for course content (normally last three modules) covered after MSE.

Course Contents:

Module 1:MOS Transistor	**Hrs.**
MOS transistor theory, MOS under static conditions, Secondary effects, Technology Scaling	**4**
Module 2:CMOS Inverter	**Hrs.**
CMOS inverter, Static and Dynamic behaviour of CMOS inverter, Power and Energy-Delay, Impact of technology scaling on inverter	**6**
Module 3 :Combinational Static Logic Design	**Hrs.**
Combinational static logic designs in CMOS, CMOS (Inverter and Complex gates), pseudo-nmos, pass-transistor logic, transmission gate logic and design aspects for optimizing the performance	**8**
Module 4 :Combinational Dynamic Logic Design	
Combinational dynamic logic designs using pre-charge evaluate logic, domino logic, np-CMOS logic , design aspects for optimizing the performance, Comparison of static and dynamic designs	
Module 5:Sequential Logic Design	**Hrs.**
Timing metrics of sequential circuits, Sequential logic designs in CMOS, Static and dynamic latches and registers	**8**
Module 6:Timing Issues in Digital Circuits	**Hrs.**
Timing Classification, Synchronous Design (Clock skew, Jitter, Clock Distribution), Self-Timed Circuits Design, Synchronizers and arbiters, Using PLL for clock synchronization	**7**

Module wise Measurable Students Learning Outcomes :

Module 1: ALL MOS map to CO1

1. MO1.1: Explain the behaviour of MOS transistor under different biasing conditions
2. MO1.2: Compare between short channel and long channel MOS transistors.
3. MO1.3: Derive the expressions for the equivalent resistance during charging and discharging of the load capacitor.
4. MO1.4: Explain the contribution of various built-in capacitances to the intrinsic load capacitance of the transitor
5. MO1.5: Solve numerical problems based on current-voltage relation under different biasing conditions.

Module 2:

1. MO2.1:Deduct the Voltage Transfer Curve for a CMOS inverter by considering the series combination of pMOS and nMOS transistor and their I-V characteristics in different regions of operation.
2. MO2.2: Derive the analytical expression for switching voltage for CMOS inverter.
3. MO2.3: Explain the piecewise linear model for VTC and derive the expressions for switching threshold (VM), Limiting values of low and high input voltage VIH, VIL, Noise margins corresponding to LOW and HIGH state viz.NMH and MNL
4. MO2.4: Compute the various parasitic capacitances and explain the transient behavior of the inverter in terms of propagation delays.
5. MO2.5: Design the dimensions of NMOS and PMOS transistors of an inverter and chain of inverters to optimize the delay and hence spped.
6. MO2.6: Compute the various components of power dissipation in inverter and optimize the dimensions for optimum energy, power delay and energy delay product.
7. MO2.7: Choose an appropriate low power approach for designing inverters with power

optimization.

Module 3:

1. MO3.1: Design a complementary MOS circuit for a given Boolean function
2. MO3.2: Compute the intrinsic delay by considering the logical and electrical effort and design the dimensions of transistors in the pull-up and pull-down network of the circuit for optimizing the performance.
3. MO3.3: Explain the design techniques for large fan-in combinational circuits.
4. MO3.4: Compute the switching factor and hence dynamic power dissipation for CMOS combinational circuits using probabilistic models.
5. MO3.5: Choose appropriate design approach to reduce switching factor and hence dynamic power dissipation.
6. MO3.6: Develop and design combinational circuits using static styles such as Pseudo-nMOS, Dynamic Switch Cascode Switch Logic (DCVSL), Pass Transistor logic (PL), Complementary Pass Transistor Logic (CPL) and Transmission Gate (TG)Logic.

Module 4:

1. MO4.1: Develop and design combinational circuits using dynamic logic static styles such as Precharge-Evaluate and explain the benefits of this for performance (speed and power) over static logic style.
2. MO4.2: Suggest the solutions to solve the problem of charge leakage, charge sharing, capacitive coupling in dynamic logic circuits.
3. MO4.3: Develop domino CMOS logic and np-CMOS logic, to solve the problem of cascading dynamic logic gates,
4. MO4.4: Select an appropriate CMOS logic style for implementation of CMOS circuits to optimize the performance for speed, area and power.

Module 5:

1. MO5.1: Explain with waveforms the timing metrics of latches and registers.
2. MO5.2: Design static latch and static register using master slave configuration and explain the difference between the two with the help of waveforms
3. MO5.3: Design dynamic latch and dynamic register using pass transistor, transmission gate and solve the problems associated with that logic style.
4. MO5.4: Develop the registers in other logic style viz. C2MOS, Dual Edge Registers, TSPCR etc to improve the performance.
5. MO5.5: Develop the schematics for SR flipflop, Schmitt Trigger, Monostable circuit, Ring Oscillator etc and explain their operation

Module 6:

1. MO6.1: Explain the timing basics of pipelined synchronous circuits and derive the restriction on clock period considering skew and jitter in clock signal.
2. MO6.2: Suggest various clock distribution approaches to minimize the clock skew and jitter problem
3. MO6.3: Develop self timed pipelined circuits by considering the physical and logical ordering of the functional and hand shaking circuit blocks and generating the appropriate hand shake signals.
4. MO6.4: Implement two-phase and four-phase protocol for data communication in self timed circuit

using Muller-C element

5. MO6.5: Design CMOS synchronizers and arbiters for robust operation of synchronous circuits.
6. MO6.6: Compute the reliability figures of CMOS synchronous circuits by taking into considerations the clocking frequency and register related manufacturing parameters.

Title of the Course and Course Code:	L	T	P	Cr
Professional Elective I:Information Theory and Coding 4EN512	3	0	0	3

Pre-Requisite Courses: Probability Theory , Digital Communication

Textbooks:

1. Thomas Cover, Joy Thomas, "*Elements of Information Theory"*, Wiley Publications, second edition.
2. Andre Neabauer, "*Coding Theory: Algorithms, Architectures & Applications*", Wiley Publications, 2010.
3. R Bose, "*Information Theory, Coding and Cryptography*", TMH 2007

References:

1. Simon Haykin*, "Digital Communication"*,Wiley Publications, second edition
2. Jorge Castineira, Moreira,"*Essentials of Error Control Coding*",Wiley, 2006
3. NPTEL lecture series on – "Information theory and coding"

Course Objectives :

1. To discuss in detail about information theory which allows us to analyze and characterize the fundamental limits on communication systems.
2. To explain various approaches of error control coding techniques.

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive Level	Bloom's Cognitive Descriptor
CO1	Analyse performance of channel using information theory.	Analyzing	Integrate
CO2	Illustrate various source coding technique.	Applying	Implement
CO3	Discuss error control coding techniques to improve performance of system.	Evaluating	Estimate

CO – PO Mapping :

PO	1	2	3	4	5	6
CO1	1					
CO2			2			
CO3				2		
3-H, 2-M, 1-L						

Assessment:

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weightage respectively.

Assessment	Marks
ISE 1	10
MSE	30
ISE 2	10
ESE	50

ISE 1 and ISE 2 are based on assignment, oral, seminar, test (surprise/declared/quiz), and group discussion.[One assessment tool per ISE. The assessment tool used for ISE 1 shall not be used for ISE 2]
MSE: Assessment is based on 50% of course content (Normally first three modules)
ESE: Assessment is based on 100% course content with70-80% weightage for course content (normally last three modules) covered after MSE.

Course Contents:

Module 1 : Review of Probability Theory	**Hrs.**
Random Variable, cumulative distribution function, probability density function, random variable, Bivariate random variable, joint and conditional probabilities.	**5**
Module 2: Entropy, Relative Entropy, and Mutual Information	**Hrs.**
Entropy, Joint Entropy and Conditional Entropy, Relative Entropy and Mutual Information, Measure of Information. Avg. and Mutual Information. Joint and conditional entropy, Rate of Information	**5**
Module 3 : Source Coding and Data Compression	**Hrs.**
Need, Source coding theorem, fixed length coding, variable length coding, kraft Inequality, Huffman Codes, Optimality of Huffman Codes, Shannon- Fanno coding technique, comparative study of source coding technique	**6**
Module 4: Channel Capacity	**Hrs.**
Discrete memoryless source, Symmetric Channels, Properties of Channel Capacity, Jointly Typical Sequences, Channel Coding Theorem, BE-SNR Trade off Fano's Inequality and the Converse to the Coding Theorem, Error Free Communication Over Noisy Channel, Binary Symmetric Channel and Introdution to Continous Sources and Channels	**8**
Module 5 : Linear Binary Block Codes	**Hrs.**
Introduction, Generator and Parity-Check Matrices, Repetition and Single-Parity-Check Codes, Binary Hamming Codes, Error Detection with Linear Block Codes, Weight Distribution and Minimum Hamming Distance of a Linear Block Code, Hard-decision and Soft-decision Decoding of Linear Block Codes, Cyclic Codes, Parameters of BCH and RS Codes, Interleaved and	**8**

Concatenated Codes	
Module 6 : Convolutional Codes	**Hrs.**
Convolutional codes – code tree, trellis, state diagram - Encoding – Decoding: Sequential search and Viterbi algorithm – Principle of Turbo coding	**8**

Module wise Measurable Students Learning Outcomes :

Module 1: Solve numerical on probability theory.

Module 2: Analyse source statistics using fundamentals of information theory

Module 3: Implement different source coding technique.

Module 4: Analyse performance of communication system using channel statistics

Module 5 and 6: Apply error control coding and decoding technique to improve performance of the system.

Title of the Course and Course Code:	**L**	**T**	**P**	**Cr**
Professional Elective 2:Biomedical Signal Processing 4EN515	3	0	0	3

Pre-Requisite Courses: Signals and Systems, Digital Signal Processing

Textbooks:

1. Reddy D C. "*Modern Biomedical Signal Processing – Principles and Techniques*", TMH, New Delhi, 2005
2. Eugene N. Bruce, "*Biomedical Signal Processing and Signal Modeling*", A Wiley-Interscience Publication JOHN WILEY & SONS, INC.

References:

1. Akay M. "*Biomedical Signal Processing*", Academic press, California,1994.
2. Bronzino J D "*The Biomedical Engineering handbook*", CRC and Free press, Florida, 1995.

Course Objectives :

1. To study origins and characteristics of some of the most commonly used biomedical signals including ECG, EEG, evoked potentials, and EMG.
2. To explore application of established engineering methods to complex biomedical signals problems

Course Learning Outcomes:

CO	**After the completion of the course the student should be able to -**	Bloom's Cognitive	
		Level	Descriptor
CO1	Apply signal processing techniques to biomedical signals	3	Applying

CO2	Analyze ECG and EEG signal with characteristic feature points.	4	Analyzing
CO3	Model a biomedical system.	6	Creating

CO – PO Mapping :

PO	1	2	3	4	5	6
CO1			2			
CO2				2		
CO3						1
3-H, 2-M, 1-L						

Assessments :

Teacher Assessment:

Two components of In Semes Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) havin 0%, 30% and 50% weights respectively.

Assessment	Marks
ISE 1	10
MSE	30
ISE 2	10
ESE	50

ISE 1 and ISE 2 are based on assignment/declared test/quiz/seminar etc.
MSE: Assessment is based on 50% of course content (Normally first three modules)
ESE: Assessment is based on 100% course content with60-70% weightage for course content (normally last three modules) covered after MSE.

Course Contents:	
Module 1 : Introduction to Biomedical Signals	**Hrs.**
Introduction to Biomedical Signals, The nature of Biomedical Signals, Examples of Biomedical Signals, Objectives and difficulties in Biomedical analysis, Signal Conversion Systems, Conversion requirements for biomedical signals, Signal conversion circuits. Application areas of Bio -Signal analysis – EEG, ECG, Phonocardiogram, Spiro Gram, Evoked Signals.	**7**
Module 2 : Signal Averaging and Data Compression Techniques	**Hrs.**
Basics of signal averaging, signal averaging as a digital filter, a typical averager, software for signal averaging, limitations of signal averaging. Turning point algorithm, AZTEC algorithm, Fan algorithm, Huffman coding	**6**
Module 3 : Adaptive Noise Cancellation	**Hrs.**
Adaptive interference / Noise cancellation: Types of noise in biosignals; Digital filters - IIR and FIR - Notch filters - Optimal and adaptive filters. Weiner filters - steepest descent algorithm - LMS adaptive algorithm - Adaptive noise canceller - cancellation of 50 Hz signal in ECG - Cancellation of maternal ECG in foetal electrocardiography.	**6**
Module 4 : Cardiological signal processing	**Hrs.**
Basic Electrocardiography, ECG data acquisition, ECG lead system, ECG signal characteristics (parameters and their estimation), Analog filters, ECG amplifier, and QRS detector, Power spectrum of the ECG, Bandpass filtering techniques, Differentiation techniques, Template matching techniques, A QRS detection algorithm, Realtime ECG processing algorithm, ECG interpretation, ST segment analyzer, Portable arrhythmia monitor.	**7**
Module 5 : Neurological signal processing	**Hrs.**
Neurological signal processing: The brain and its potentials, The electrophysiological origin of brain waves, The EEG signal and its characteristics (EEG rhythms, waves, and transients), Correlation. Analysis of EEG channels: Detection of EEG rhythms, Template matching for EEG, spike and wave detection	**6**
Module 6 : Modeling of Biomedical Systems	**Hrs.**
Motor unit firing pattern, Cardiac rhythm, Formants and pitch of speech, Point process, Parametric system modeling, Autoregressive model, Autocorrelation method, Application to random signals, Computation of model parameters, Levinson-Durbin algorithm, Computation of gain factor,	**8**

Covariance method, Spectral matching and parameterization, Model order selection, Relation between AR and Cepstral coefficients.	

Modulewise Measurable Students Learning Outcomes :
After completion of respective modules, Students will be able to -
Module 1: gain insight into different biomedical signals
Module 2 & 3: get introduced to signal processing techniques to improve biomedical signals
Module 4 & 5 : understand applications of signal processing in Cardiology and Neurology
Module 6: design algorithm for modeling of biomedical systems.

Title of the Course and Course Code: **Professional Elective 2:Embedded Linux Programming 4EN516**	**L**	**T**	**P**	**Cr**
	3	0	0	3

Pre-Requisite Courses: Nil

Textbooks:

1. Christopher Hallinan, *"Embedded Linux Primer: A Practical Real-World Approach",* Prentice Hall; 1st edition (September 28, 2006), ISBN 978-0137017836
2. Richard Stones, Neil Matthew, *"Beginning Linux Programming"*, Wiley; Fourth edition (2008)
3. Felix Alvaro, "LINUX: Easy Linux For Beginners", Amazon.com
4. Karim Yaghmour, Jon Masters, Gilad Ben-Yossef, Philippe Gerum, *"Building Embedded Linux Systems",* O'Reilly Media; Second Edition (August 22, 2008) ISBN: 978-0596529680

References:

1. P. Raghavan, Amol Lad, Sriram Neelakandan, *"Embedded Linux System Design and Development",* Auerbach Publications; 1 edition (December 21, 2005), ISBN: 978-0849340581
2. http://crashcourse.ca/introduction-Linux-kernel-programming-2nd-edition
3. Anand Iyer, Director, Calypto Design Systems, NPTEL Course: "*Linux Programming & Scripting*", by Online Course on YouTube and Also on http://nptel.ac.in, L1-4, L7 and L43

Course Objectives :

1. To make students familiar with installation and use of the embedded Linux operating system
2. To facilitate the students to learn the fundamentals of Linux as applied to embedded hardware
3. To give exposure to system design using embedded Linux as per the industry trends.

CO-PO Mapping : Use H: High **M:** Moderate **L:**Low **for mapping;**

PO	**1**	**2**	**3**	**4**	**5**	**6**
CO1			2			
CO2				2		
CO3						1
3-H, 2-M, 1-L						

Assessments

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weights respectively.

ISE 1: 10 Marks to be submitted before MSE marks. It is open to students.

ISE 2: 10 Marks to be submitted before ESE. It is hidden component for students.

MSE: 30 Marks to be submitted within 10 days after MSE examination is over
(Generally on module 1-3)

ESE: 50 Marks to be submitted within 10 days after ESE examination
(60-70% weight for module 4-6 and 30-40% on module 1-3)

Course Contents:

Module 1: Introduction	**Hrs.**
Introduction to Linux, Linux Distributions, Open source Software, GPL, Facilities in Embedded Linux Boards used in Industry/Market, Important Accessories of Linux boards available/used in industry, Care to take in handling the Linux boards, Development Setup for EL, OS installation, init process, initrd, boot loaders, lilo and GRUB boot loaders, Case studies of Embedded Linux Based Systems	**5**
Module 2: Linux file system and commands	
Linux File System, Permissions, CLI and Linux Shells, Linux Commands, Linux concepts, Shell Script, Basic Linux system administration tasks on the RPi. Linux commands for file and process management. Linux Programming, Multi-file C programming Using make utility, Makefile, GNU debugger. Transferring Files Between Systems**,** Kernel, building kernel image.	**6**
Module 3: Multithreading and Hardware Access:	
Threads and processes, Multithreaded C programming. EL hardware design issues, Logic-level translation circuitry. Case studies of hardware of frequently used interfaces, Communication with EL board through network, EL GPIO control using sysfs, wiringPi and python. Python libraries	**7**
Module 4: Hardware Interfacing and Programming-I	
Using onboard I2C, SPI, and UART capabilities. Circuits to the RPi that interface to its I2C bus, Linux I2C-tools. Communicate between UART devices using both Linux tools and custom C or Python code. Interface to a low-cost GPS sensor using a UART connection. Extend the input/output capability using external serial ADCs, DACs, Increase the number of available GPIOs on the RPi using both I2C and SPI GPIO expanders.	**7**
Module 5: Hardware Interfacing and Programming-II	
Using Interrupt functionality on devices. Increasing the number of available serial UART devices on the RPi using low-cost USB-to-TTL devices. USB Bluetooth adapter for the RPi and connect to it from a mobile device for the purpose of building a basic remote-control application. Using Wi-Fi and Xigbee along with EL board. Hardware design for given system specifications.	**7**
Module 6: Basic Image Processing on Embedded Linux:	
Camera interfacing to EL board, Capture image and video. Stream video data to the Internet using Linux applications and UDP, multicast, and RTP streams. Using OpenCV to perform basic image processing on the RPi. Use OpenCV to perform a computer vision face-detection task. Play audio data on the using HDMI audio and USB audio adapters.	**7**

Module wise Measurable Students Learning Outcomes:

At the end of each module the students will be able to,

Module 1: Apply the basic concepts of Linux for various case studies.

Module 2: Apply the basic and frequently required Linux commands and shell scripting for basic administration

Module 3: Write, compile multi-file, multi-threaded programs using make and debug using gdb.

Module 4: Write programs to access and control the on board as well as outside hardware such as such as I2C/SPI/ GPIO/ Keyboard/LCD/Serial port etc. Design external hardware for EL board.

Module 5: Write programs for extending EL hardware and modules such as Wi-Fi module.

Module 6: Write OpenCV program for basic image processing using Linux.

Title of the Course and Course Code: Electronics Lab 2 4EN552	L	T	P	Cr
	0	0	4	2

Pre-Requisite Courses: Digital VLSI Design Lab

Reference Books:

1. Cadence manual
2. Microwind manual
3. Lab General manual

Course Objectives:

1. Demonstrate the flow of following EDA tools for designing digital circuits
   a. Microwind for designing digital circuits at physical level
   b. Cadence flow (Schematic entry to simulation) for implementing CMOS digital circuits
2. Prepare the students for executing an individual or group problem of medium complexity.

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive	
		Level	Descriptor
CO1	**Design** and **Simulate schematics** of CMOS circuits using Cadence tools and 90 nm technology	6^{th} (Creating)	Design and Simulate PO3
CO2	Design and simulate physical layouts with optimum area for gates, pass-T, TX gates etc using microwind tools	6^{th} (Creating)	
CO3	**Formulate** a research a problem, design, build and simulate either a researched problem or assigned by the supervisor in Digital VLSI Design area independently, submit a written report in standard format and demonstrate the simulation results with justification.	6^{th} (Creating) Skills viz. Research Life long learning & communication skills and ethics	

CO-PO Mapping :

PO	1	2	3	4	5	6
CO1			3			
CO2				3		
CO3	**2**					
3-H, 2-M, 1-L						

Lab Assessment:

There are four components of lab assessment, LA1, LA2, LA3 and Lab ESE.
IMP: Lab ESE is a separate head of passing.

Assessment	Based on	Conducted by	Conduction and Marks Submission	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 4 Submission at the end of Week 5	25
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 5 to Week 8 Submission at the end of Week 9	25
LA3	Lab activities, attendance, journal	Lab Course Faculty	During Week 10 to Week 14 Submission at the end of Week 14	25
Lab ESE	Lab Performance and related documentation	Lab Course faculty	During Week 15 to Week 18 Submission at the end of Week 18	25

Week 1 indicates starting week of Semester.
Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments.

Proposed List of experiments:

A: Using cadence Design Tools:

1. NMOS and PMOS characterization
2. Implementation of CMOS inverter and its characterization for VTC and power
    a. Equal area approach
    b. Equal delay approach
3. Implementation of 2-inpout NAND and NOR
    a. Finding out rise time, fall time of the output and propagation delay (50% input to
    b. 50% output) High-to-Low and Low-to-High
    c. Comparison of both for delay and power
4. Implementation of 1-bit full adder using carry-out of the stage to drive the sum output (28 transistor implementation)
5. Implementation of 2-input NAND and NOR gates using different logic styles and compare the performance parameters with complementary CMOS logic style
    a. Pseudo logic style
    b. Pass Transistor logic style
    c. Transmission gate logic style
    d. Differential cascade voltage switch logic
    e. Dynamic (pre-charge and evaluate) logic style
6. Implementation of transmission gate based full adder circuit
7. Implementation of four bit Manchester carry chain
8. Implementation of 4-bit barrel shifter using pass transistors

B. Demonstration of Microwind tool for layout by explaining DRC and simulation,

9. Implementation of inverter, 2 input NAND gate and any other circuit for practice

C. Task/miniproject/research problem:

For the last lab session which students will have to carry out a task for a period of at least six weeks it is recommended that:

1. Student can search or teacher can assign a course related medium complexity task to a group of student not exceeding two by defining the problem statement suitably.
2. Student has to submit a report/Journal consisting of appropriate documents – Abstract, Certificate of Completion by the supervisor, Table of Contents, Abbreviations, and other sections/chapters viz. Introduction, Motivation, Objectives, Outcomes, Brief theoretical Background, Problem Analysis, Design Aspects, Algorithms, Mathematical Model, Test Strategy, Results, Result Analysis and Conclusions and Future Scope) in the institute level standard format.
3. Cadence tools or other similar EDA tools are to be used for designing and implementing the designs and the report is to be written in standard IEEE format preferably using Latex.

Semester II

Title of the Course and Course Code :	L	T	P	Cr
Advanced Embedded Programming 4EN521	3	0	0	3

Pre-Requisite Courses: Embedded System Design

Textbooks:

1. The Real-Time Kernel by Micrium
2. Real-time Operating Systems: Book 1 - The Theory (The engineering of real-time embedded systems) by Jim Cooling

   Embedded Systems: Introduction to Arm® Cortex™-M Microcontrollers , Fifth Edition (Volume 1) by Jonathan W Valvano

References: http://www2.keil.com/mdk5/cmsis/

User Guide and Reference Guide of LPC 1768, STM32F7

www.usb.org › Developers › Documents

https://www.segger.com/

Course Objectives :

To illustrate Real Time operating system with multi-tasking
To illustrate task synchronisation of various tasks
To develop student in latest Buses Like USB, Ethernet
To develop student to design GUI Applications

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive Level	Bloom's Cognitive Descriptor
CO1	Apply RTOS concepts and multitasking to embedded systems	Applying	Apply
CO2	Design RTOS based systems with Process Synchronization using semaphore, mutex , flags, messages etc.	Creating	Design
CO3	Explain Advance multi-core processing systems and inter processor communication.	Evaluating	Explain
CO4	Design embedded GUI based system	Creating	Design
CO5	Develop embedded programs with embedded USB port	Creating	Develop

CO6	Create embedded system using various IO peripherals	Creating	Create

CO-PO Mapping :

PO	1	2	3	4	5	6
CO1			2			
CO2				3		
CO3						2
CO4				2		
CO5			2			
CO6	1		2			
3-H, 2-M, 1-L						

Assessment:

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weightage respectively.

Assessment	Marks
ISE 1	10
MSE	30
ISE 2	10
ESE	50

ISE 1 and ISE 2 are based on assignment, oral, seminar, test (surprise/declared/quiz), and group discussion.[One assessment tool per ISE. The assessment tool used for ISE 1 shall not be used for ISE 2]
MSE: Assessment is based on 50% of course content (Normally first three modules)
ESE: Assessment is based on 100% course content with70-80% weightage for course content (normally last three modules) covered after MSE.

Course Contents:

Module 1: RTOS Programing	**6 Hrs.**
Need and Requirements of RTOS, Concept of Multitasking, Priority inversion, RTOS structure, TCB block design, Repetitive Timer Requirement, Memory Requirement for each Task	
Module 2 : RTOS Process Synchronization	**6 Hrs.**
System events and interrupts. Task synchronization with Flags, Semaphore, Mutex. Inter process communication with Messages queue/ MailBox	
Module 3 : Multi core processors	**6 Hrs.**
Programming on Multi core processors, inter-core communication, interrupt handling, software architecture for multi core processors.	
Module 4: GUI Programming	**6 Hrs.**
Graphical Display Interface, Touch Screen Interface, Graphic Display drivers, GUI API calls for Windows, Dialogs programming, Designing Menu, Widgets programing for Textbox, Label, Combo box etc. Designing Application with GUI	
Module 5: USB Programming	**6 Hrs.**
USB 2.0 specifications, USB block diagram, Device , Host Interface, concept of endpoint, Data transfer on USB bus, Various USB data transfers, API for USB Host and Device Programming, Writing Application with USB Host and Device	
Module 6 : Ethernet Programming & Embedded Application	**6 Hrs.**

Motivation, Ethernet Interface , API for Ethernet Programming, Writing Server Application with Ethernet interface. Designing Server Application with GUI	

Module wise Measurable Students Learning Outcomes : Students will able to

Module 1: Apply RTOS concepts and multitasking to embedded system

Module 2: Design RTOS based embedded system with Process Synchronization using semaphore, mutex, flags, messages etc.

Module 3: Design embedded system with Advance peripherals like USB, Graphics displays, Ethernet etc.

Module 4: Design GUI based system

Module 5: Develop programs with USB port

Module 6: Design embedded system applications using various peripherals

Title of the Course and Course Code:	**L**	**T**	**P**	**Cr**
Advanced Communication Networks and IoT 4EN522	3	0	0	3

Pre-Requisite Courses: Data Communication and Networking

Textbooks:

1. D.E. Comer *"Internetworking with TCP/IP*", Vol. I (4th Edition), II, III (PHI)
2. *"Internet of Things Applications and Protocols ", Wiely publication 2nd Ed.*
3. William Stallings "*Foundations of Modern Networking : SDN, NFV, QoE, IoT and Cloud"* Pearson Education

References:

1. Richard Steven "*UNIX Network Programming: III Edition*", , PHI
2. Stevens, Gabrani *" TCP/ IP illustrated Vol1, 2*" PEARSON
3. Leon-Garcia, Widjaja, "Communication Networks", TMH.

Course Objectives :

1. To provide understanding of the networking concepts and widely used protocol suite TCP/IP in detail
2. To demonstrate Policy, Procedure and Managerial approach towards a required Network design and application program.
3. To expose the student with the latest trends & techniques in the field and expertise him/her considering academic & professional aspect**.**

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive	
		Level	**Descriptor**
CO1	Explain in a concise manner how the general Internet as well as Internet of Things work.	Understanding, Analysing	Explain, Identify
CO2	Design prototype to demonstrate Internet of Thing application with constraints and opportunities of network.	Creating	Design
CO3	Apply the knowledge for solution building	Applying	Demonstrate, Apply

CO-PO Mapping :

PO	1	2	3	4	5	6
CO1			3			
CO2				3		
CO3	2					
3-H, 2-M, 1-L						

Assessment:

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weightage respectively.

Assessment	Marks
ISE 1	10
MSE	30
ISE 2	10
ESE	50

ISE 1 and ISE 2 are based on assignment, oral, seminar, test (surprise/declared/quiz), and group discussion.[One assessment tool per ISE. The assessment tool used for ISE 1 shall not be used for ISE 2]

MSE: Assessment is based on 50% of course content (Normally first three modules)

ESE: Assessment is based on 100% course content with70-80% weightage for course content (normally last three modules) covered after MSE.

Course Contents:

Module 1 Introduction to Internet Technology	**Hrs.**
Internet addresses, ARP, RARP, Tools of Internet access and addressing , Routing Features of Ipv6, General form of an Ipv6 address types, Proposed Ipv6 address space, ICMP.	**6**
Module 2 Transport Layer TCP	**Hrs.**
UDP, TCP, TCP state diagram, Flow, Error Congestion Control in TCP, TCP Timers, Kern's algorithm, UDP TCP Socket	**7**
Module 3 Internet Applications and Protocols	**Hrs.**
Real time transport protocol (RTP), RSVP, Encapsulation, Session Control Protocols DNS techniques DNS: Names for machines, Remote Login: Remote Interactive computing, TELNET protocol, FTP: File access and transfer, Online shared access, sharing by file transfer, SMTP, Electronic Mail, Standards for Services.	**6**
Module 4 Internet Security	**Hrs.**
Firewall, mechanisms for internet security, A firewall, the details of firewall architecture, Types of fire walls, IPSec, VPN.	**6**
Module 5 IoT	**Hrs.**
IoT definitions: overview, applications, potential & challenges, and architecture. M2M Protocols for Sensor Networks. IoT CASE Study.	**6**
Module 6 Cloud and SDN	**Hrs.**
Introduction to Cloud Computing including benefits, challenges, and risks Cloud Computing Models. SDN: Introduce software defined networking: the background, the development, and the challenges.	**7**

Module wise Measurable Students Learning Outcomes :

Module 1: Demonstrate basic IoT concept
Module 2: Analyse TCP/IP protocol
Module 3: Analyse the Application layer protocols and applications
Module 4: Illustrate different security issues and mitigation technique
Module 5 : Design prototype IOT system
Module 6: Explain advanced systems and overview of IoT from design and analysis prospective.

Title of the Course and Course Code:	**L**	**T**	**P**	**Cr**
Electronics Lab 3 4EN571	0	0	4	2

Pre-Requisite Courses: Embedded System Design

Textbooks:

3. The Real-Time Kernel by Micrium
4. Real-time Operating Systems: Book 1 - The Theory (The engineering of real-time embedded systems) by Jim Cooling

Embedded Systems: Introduction to Arm® Cortex™-M Microcontrollers , Fifth Edition (Volume 1) by Jonathan W Valvano

References: http://www2.keil.com/mdk5/cmsis/

User Guide and Reference Guide of LPC 1768, STM32F7

www.usb.org › Developers › Documents

https://www.segger.com/

Course Objectives :

To illustrate Real Time operating system with multi-tasking
To illustrate task synchronisation of various tasks
To develop student in latest Buses Like USB, Ethernet
To develop student to design GUI Applications

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive Level	Bloom's Cognitive Descriptor
CO1	Apply RTOS concepts and multitasking to embedded systems	Applying	Apply
CO2	Design RTOS based systems with Process Synchronization using semaphore, mutex , flags, messages etc.	Creating	Design
CO3	Explain Advance multi-core processing systems and inter processor communication.	Evaluating	Explain
CO4	Design embedded GUI based system	Creating	Design
CO5	Develop embedded programs with embedded USB port	Creating	Develop
CO6	Create embedded system using various IO peripherals	Creating	Create

CO-PO Mapping :

PO	1	2	3	4	5	6
CO1			2			
CO2				2		
CO3				2		
CO4	2					
3-H, 2-M, 1-L						

Lab Assessment:

There are four components of lab assessment, LA1, LA2, LA3 and Lab ESE.
IMP: Lab ESE is a separate head of passing.

Assessment	Based on	Conducted by	Conduction and Marks Submission	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 4 Submission at the end of Week 5	25
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 5 to Week 8 Submission at the end of Week 9	25
LA3	Lab activities, attendance, journal	Lab Course Faculty	During Week 10 to Week 14 Submission at the end of Week 14	25
Lab ESE	Lab Performance and related documentation	Lab Course faculty	During Week 15 to Week 18 Submission at the end of Week 18	25

Week 1 indicates starting week of Semester.
Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments.

Module wise Measurable Students Learning Outcomes : Students will able to create and demonstrate programs for

Module 1: RTOS multitasking for embedded system

Module 2: Process Synchronization using semaphore, mutex, flags, messages etc.

Module 3: Designing GUI based system

Module 4: Ethernet peripherals

Module 5: USB Host Controller port

Module 6: USB device port

Module 7: Camera interface peripherals

Module 8: Design embedded system applications using GUI

Title of the Course and Course Code:	**L**	**T**	**P**	**Cr**
Industrial Project Lab 4EN572	0	0	4	2

Course Objectives :

1.To explore the basic principles of communication (verbal and non-verbal) and active, empathetic listening, speaking and writing techniques.

2. To Identify, understand and discuss current, real-world issues, new technologies, research, products, algorithms etc.

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive Level	Bloom's Cognitive Descriptor
CO1	To use multiple thinking strategies to examine real-world issues and explore creative possibilities of expression	Analyzing	Identify, Examine
CO2	To acquire, articulate, create and convey intended meaning using verbal and nonverbal method of communication	Creating	Produce, Create
CO3	To learn and integrate, through independent learning in technologies, with disciplinary specialization in Electronics Engineering	Creating	Develop, Organize, Prepare

CO-PO Mapping :

PO	1	2	3	4	5	6
CO1				3		
CO2			3			
CO3						2
3-H, 2-M, 1-L						

Lab Assessment:

There are four components of lab assessment, LA1, LA2, LA3 and Lab ESE.
IMP: Lab ESE is a separate head of passing.

Assessment	Based on	Conducted by	Conduction and Marks Submission	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 4 Submission at the end of Week 5	25
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 5 to Week 8 Submission at the end of Week 9	25
LA3	Lab activities, attendance, journal	Lab Course Faculty	During Week 10 to Week 14 Submission at the end of Week 14	25
Lab ESE	Lab Performance and related documentation	Lab Course faculty	During Week 15 to Week 18 Submission at the end of Week 18	25

Week 1 indicates starting week of Semester.
Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments.

Course Contents:

The student shall have to deliver the seminar on a topic approved by guide and authorities. It is recommended that seminar shall be on the topic relevant to state-of-the-art trends in the field of Electronics Engineering, preferably on the topic of specialization based on the electives selected or domain of interest.

It is appreciated and strongly recommended that the student will select the domain of his/her dissertation and identify the literature confined to the domain. Thorough literature study based on the broad identified topic has to be carried out. This preparation will ultimately lead to convergence of the efforts for the dissertation work to be completed in Semester III and IV.

The relevant literature then be explored as high-tech, exotic, recent technological advancements, future trends, applications and research & innovations. Multidisciplinary topics are encouraged. The student shall submit the duly approved and certified seminar report in standard format, for satisfactory completion of the work by the concerned Guide and head of the department. The student will be assessed based on his/her presentation and preparations by the panel of examiners in the department.

Title of the Course and Course Code :	**L**	**T**	**P**	**Cr**
Professional Elective 3: RTL Simulation and Synthesis with PLDs 4EN531	3	0	0	3

Pre-Requisite Course: Digital Design Principles

Textbooks:

1. *"Richard Sandige,: Modern Digital Design \, MGH, International Edition*
2. *"Donald D. Givone, "Digital Principles and Design", TMH*
3. *Charles Roth, Jr Lizy K John, "Digital System Design using VHDL", Cengage*

References:

1. *"Xilinx Simulation and Synthesis Guide" www://Xilinx.com*
2. *Net material on simulation and synthesis from Xilinx, Altera, etc*

Course Objectives:

1. Explain the concepts of HDL simulation and synthesis
2. Illustrate with examples good ways of writing synthesizable HDL code
3. Guide the students to explore various FPGA architectures and compare those
4. Explain the concepts of testing and testability
5. Facilitate students to develop their own IP for a given problem and use in typical application.

Course Learning Outcomes:

At the end of the course student will be able to

CO1: Model and write synthesizable code for digital circuits using VHDL/Verilog

CO2: Justify FPGA architecture for a specific vendor

CO3: Explain the design flow and design combinational and sequential circuits using FPGA technology
CO4: Differentiate between functional and timing simulation
CO5: Design the digital systems with built-in testability aspect
CO6: Design prototypes and IPs for given problem.

CO-PO Mapping :

PO	1	2	3	4	5	6
CO1			2			
CO2			2			
CO3				2		
CO4			2			
CO5	3					
CO6	3					
3-H, 2-M, 1-L						

Assessment:

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weightage respectively.

Assessment	Marks
ISE 1	10
MSE	30
ISE 2	10
ESE	50

ISE 1 and ISE 2 are based on assignment, oral, seminar, test (surprise/declared/quiz), and group discussion.[One assessment tool per ISE. The assessment tool used for ISE 1 shall not be used for ISE 2]
MSE: Assessment is based on 50% of course content (Normally first three modules)
ESE: Assessment is based on 100% course content with70-80% weightage for course content (normally last three modules) covered after MSE.

Course Contents:

Module Details	Hrs
Module 1: Top Down approach to design digital systems, FPGA design flow, Design of FSMs and ASMs, Clock issues, Metastability, Multi-clock domain designs (CO1,	**6**
Module 2: RTL code design entry using VHDL/Verilog and correct design hierarchy, VHDL Simulation, Functional simulation, (CO1, CO4)	**6**
Module 3: Generics and constants, Data path designs, FSM design styles, Designing memories, Designing arithmetic blocks, VHDL/Verilog Attributes (CO3)	**8**
Module 4: Programmable Logic Devices, FPGA Architecture, VHDL Synthesis, timing simulation, Static timing analysis, Placement (floor planning), Clock tree synthesis, Routing, Downloading synthesized, placed and routed designs in FPGAs (CO2)	**8**
Module 5: Design for performance, Timing problems root causes, set-up and hold time violations, Defining constraints, Low power VLSI designs, Design for testability (CO5)	**6**
Module 6: IP and Prototyping**:** Implementing IPs for designing complex digital circuits, Speed issues and few case studies (CO6)	**6**

Module wise Measurable Students Learning Outcomes :

Module 1: CO1
Module 2: CO1, CO4

Module 3: CO3,
Module 4: CO2
Module 5: CO5
Module 6: CO6

Title of the Course and Course Code	L	T	P	Cr
Professional Elective 3 : Pattern Recognition and Image Analysis 4EN532	3	0	0	3

Pre-Requisite Courses: Signal Processing, Image Processing

Textbooks:

1. Earl Gose and Richard Johnsonbaugh Steve Jost, "Pattern Recognition and Image Analysis", PHI publication.
2. Sing Tze Bow, M. Dekker, "Pattern Recognition and Image Processing", Springer, 1992

References:

1. Rafael C. Gonzalez and Richard E. Woods, "Digital Image Processing", Addinson – Wesley.
2. M. A. SID – AHMED, "Image Processing Theory Algorithms and Architecture", McGraw Hill Inc.

Course Objectives :

To be familiar with processing of images, recognition of the pattern and their applications.

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive Level	Bloom's Cognitive Descriptor
CO 1	Contrast different image processing operations for improving image quality through enhancement, restoration and filtering etc..	Understanding	Contrast
CO 2	Categorize Image segmentation for partitioning into objects and background	Analysing	Categorize
CO 3	Analyse extraction of image features, quantifying shapes, pattern recognition, image analysis	Analysing	Analyse

CO-PO Mapping :

PO	1	2	3	4	5	6
CO1			2			
CO2				2		
CO3			2			
3-H, 2-M, 1-L						

Assessment:

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weightage respectively.

Assessment	Marks
ISE 1	10
MSE	30
ISE 2	10
ESE	50

ISE 1 and ISE 2 are based on assignment, oral, seminar, test (surprise/declared/quiz), and group discussion.[One assessment tool per ISE. The assessment tool used for ISE 1 shall not be used for ISE 2]
MSE: Assessment is based on 50% of course content (Normally first three modules)
ESE: Assessment is based on 100% course content with70-80% weightage for course content (normally last three modules) covered after MSE.

Module wise Measurable Students Learning Outcomes :

students are able to

Module 1: Compare basic of pre-processing algorithm

Module 2: Experiment with the segmentation on various images

Module 3: Choose morphological filters for various application

Module 4: Distinguish various texture in an image

Module 5: Identify various pattern in an image

Module 6: Classify pattern in an image

Title of the Course and Course Code:	L	T	P	Cr
Professional Elective 4: Wireless Sensor Networks 4EN535	3	0	0	3

Pre-Requisite Courses: Fundamentals of networking.

Textbooks:

1. Kazem Sohraby, Daniel Minoli, Taieb Znati, "Wireless Sensor Networks Technology Protocols and Applications", John Wiley & Sons Inc. Publication ,2007

References:

1.Edgar H. Callaway, Jr. and Edgar H. Callaway, "Wireless Sensor Networks: Architectures and Protocols" ,CRC Press, August 2003
2. Ian F. Akyildiz, Mehmet Can Vuran**,"**Wireless Sensor Networks" ,John Wiley & Sons Ltd. 2010

Course Objectives :

1.To explain the Wireless Sensor Network and its applications
2.To distinguish working principles of various WSN protocols
3.To discuss security issues of WSN and its performance

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive Level	Bloom's Cognitive Descriptor
CO1	Analyse Prototypes for Wireless Sensor Network	Analyzing	Distinguish
CO2	Calculate performance issues in Wireless Sensor Network	Evaluating	Justify
CO3	Analyse different layer protocols and security issues of Wireless Sensor Network	Analyzing	Identify

CO-PO Mapping :

PO	1	2	3	4	5	6
CO1				3		
CO2			3			
CO3				2		
3-H, 2-M, 1-L						

Assessment:

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weightage respectively.

Assessment	Marks

ISE 1	10
MSE	30
ISE 2	10
ESE	50

ISE 1 and ISE 2 are based on assignment, oral, seminar, test (surprise/declared/quiz), and group discussion.[One assessment tool per ISE. The assessment tool used for ISE 1 shall not be used for ISE 2]
MSE: Assessment is based on 50% of course content (Normally first three modules)
ESE: Assessment is based on 100% course content with70-80% weightage for course content (normally last three modules) covered after MSE.

Course Contents:

Module 1 :Introduction and Overview of Wireless Sensor Networks	**Hrs.**
Introduction to wireless Ad-hoc network , Mobile Ad-hoc Network and Overview of Wireless Sensor Networks, Applications of Wireless Sensor Networks	**5**
Module 2:Wireless Transmission Technology and Medium Access Control Protocols	**Hrs.**
Basic Wireless Sensor Technology, Sensor Node Technology, Hardware and Software, Sensor Taxonomy, WN Operating environment, WN Trends, Wireless Transmission Technology and Systems, Medium Access Control Protocols for Wireless Sensor Networks, Fundamentals of MAC Protocols, MAC Protocols for WSNs.	**7**
Module 3: Routing Protocols and Transport Control Protocols for Wireless Sensor Networks	**Hrs.**
Routing Challenges and Design Issues in Wireless Sensor Networks, Routing Protocols for Wireless Sensor Networks, -Data Dissemination and Gathering, , Routing Strategies in Wireless Sensor Networks, Transport Control Protocols for Wireless Sensor Networks, Traditional Transport Control Protocols, Transport Protocol Design Issues, Examples of Existing Transport Control Protocols, Performance of Transport Control Protocols	**9**
Module 4: Middleware and Network Management for WSN	**Hrs.**
WSN Middleware Principles- Middleware Architecture, Existing Middleware, Network Management for Wireless Sensor Networks Operating Systems for Wireless Sensor Networks- Operating System Design Issues, Examples of Operating Systems-TinyOS	**7**
Module 5: Security Issues	**Hrs.**
WSN security issues, Possible attacks on WSN, worm hole, black hole , sync attack and effect on performance, mitigation techniques	**6**
Module 6: Performance and Traffic Management	**Hrs.**
Performance and Traffic Management- Introduction, Background, WSN Design Issues, Performance Modelling of WSNs, Performance Metrics, Basic Models, Network Models	**5**

Module wise Measurable Students Learning Outcomes :

Module 1: Distinguish different types of ad hoc networks and its applications

Module 2: i)Analyze wireless sensor node components , transmission impairments and performance issues like power, Energy, distance between wireless nodes

ii)Analysis of MAC protocols

Module 3: i)Distinguish Routing protocols and Transport control protocol for WSN

Module 4: i)Describe of middleware and network management protocols

ii)Design issues of OS for WSN

Module 5: Identify different security issues of WSN

Module 6: Analyse Different models of WSN and its performance analysis.

Title of the Course and Course Code:	L	T	P	Cr
Program Elective 4: System On Chip 4EN536	3	0	0	3

Pre-Requisite Courses: Microprocessor / Microcontrollers

Textbooks:1. Michael J Flynn and Wayne Luk, ―Computer system Design: System-on-Chip‖, Wiley-India, 2012.
2. SudeepPasricha and NikilDutt, ―On Chip Communication Architectures: System on Chip Interconnect‖, Morghan Kaufmann Publishers, 2008.
3.Lin, Y-L S (ed.), ―Essential Issues in SOC Design: Designing Complex Systems-on-chip. Springer, 2006.

References: 1. Wolf W H, ―Computers as Components: Principles of Embedded Computing System Design‖, Elsevier, 2008.
2. Patrick Schaumont ―A Practical Introduction to Hardware/Software Co-design‖, Patrick Schaumont, Springer, 2012.
3. Lin, Y-L S (ed.), ―Essential Issues in SOC Design: Designing Complex Systems-on-chip. Springer, 2006. 6. Wayne Wolf, ―Modern VLSI Design: IP Based Design‖, Prentice-Hall India, 2009.
4. Amba bus architecture at http://www.arm.com/products/solutions/Ambahomepage.html

Course Objectives :
1. To make students aware of the system on chip concepts
2. To make students learn the Bus interconnect hardware Design approach
3. To make students learn the IP design
4. To make students learn Model-based system design
5. To make students learn hardware software co-design approach

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive Level	Descript
CO1	Illustrate the concepts of system on chip.	Illustrating	Illustrate
CO2	Design approach using interconnect bus like AMBA for SoC technology 3. They will be able to design IP using EDA Tools	Creating	Design
CO3	Design IPs using EDA Tools	Creating	Design
CO4	Design SoC for given specifications and implement using EDA Tools.	Creating	Design
CO5	Discuss the test strategy, write the test benches and test the designed SoC for functionality and performance using EDA	Creating	Discuss, Test

CO-PO Mapping :

PO	1	2	3	4	5	6
CO1			2			
CO2						1
CO3				2		
CO4						2
CO5			2			
3-H, 2-M, 1-L						

Assessment:

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weightage respectively.

Assessment	Marks
ISE 1	10
MSE	30
ISE 2	10
ESE	50

ISE 1 and ISE 2 are based on assignment, oral, seminar, test (surprise/declared/quiz), and group discussion.[One assessment tool per ISE. The assessment tool used for ISE 1 shall not be used for ISE 2]
MSE: Assessment is based on 50% of course content (Normally first three modules)
ESE: Assessment is based on 100% course content with70-80% weightage for course content (normally last three modules) covered after MSE.

Course Contents:

Module 1	**4**
INTRODUCTION TO THE CONCEPT OF SoC: Differences between Embedded systems and SOCs ,Driving Forces for SoC - Components of SoC - Design flow of SoC - Hardware/Software nature of SoC - Design Trade-offs - SoC Applications.	
Module 2	**6**
SYSTEM-LEVEL DESIGN: Processor selection-Concepts in Processor Architecture: Instruction set architecture (ISA), elements in Instruction Handing-Robust processors: Vector processor, VLIW, Superscalar, CISC, RISC—Processor evolution: Soft and Firm processors, Custom Designed processors- on-chip memory.	
Module 3	**8**
SYSTEM-LEVEL INTERCONNECTION: On-chip Buses: basic architecture, topologies, arbitration and protocols, Bus standards: AMBA, Wishbone, Avalon. Network-on-chip: Architecture-topologies-switching strategies - routing algorithms - flow control, Quality-of-Service Re-Configurability in communication architectures.	
Module 4	**6**
IP BASED SYSTEM DESIGN: Introduction to IP Based design, Types of IP, IP across design hierarchy, IP life cycle, Creating and using IP - Technical concerns on IP reuse - IP integration - IP evaluation on FPGA prototypes.	
Module 5	**6**
SOC IMPLEMENTATION: Study of processor IP, Memory IP, wrapper Design - Real-time operating system (RTOS), Peripheral interface and components, High-density FPGAs, EDA tools from Xilinx and Intel for SoC design.	

Module 6	6
SOC TESTING: Manufacturing test of SoC: Core layer, System layer, Application layer- P1500 Wrapper Standardization-SoC Test Automation (STAT).	

Module wise Measurable Students Learning Outcomes : students will

Module 1: Illustrate the SOC hardware Design approach
Module 2: Discuss various CPU architectures
Module 3: Illustrate interconnect buses
Module 4: Design Model-based SoC system with EDA tool
Module 5: Design hardware software based SOC system with EDA tool
Module 6: Develop and test SoC with sample software programs using EDA tool

Title of the Course and Course code : Electronics Lab 4 4EN573	L	T	P	Cr
	0	0	4	2

Pre-Requisite Courses: Digital design, Signal processing

Text Books: Related to respective Program Elective 2 courses

Reference Books: Related to respective Program Elective 2 courses

Course Objectives :

1. To develop student's technical skill in the course which he has chosen as Program Elective 1
2. To prepare the students for their dissertation work by assigning them mini projects

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive Level	Bloom's Cognitive Descriptor
CO1	Choose and collect required data, find solution , develop mathematical /simulation model for given assignment	Analysing	Construct, Compare
CO2	Write programs using appropriate software tool for given assignment	Creating	Propose, formulate
CO3	Develop an ability to work independently for open ended research (Dissertation) work	Creating	Design

CO-PO Mapping :

PO	1	2	3	4	5	6
CO1			2			
CO2				2		
CO3	2					
3-H, 2-M, 1-L						

Lab Assessment:

There are four components of lab assessment, LA1, LA2, LA3 and Lab ESE.
IMP: Lab ESE is a separate head of passing.

Assessment	Based on	Conducted by	Conduction and Marks Submission	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 4 Submission at the end of Week 5	25
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 5 to Week 8 Submission at the end of Week 9	25
LA3	Lab activities, attendance, journal	Lab Course Faculty	During Week 10 to Week 14 Submission at the end of Week 14	25
Lab ESE	Lab Performance and related documentation	Lab Course faculty	During Week 15 to Week 18 Submission at the end of Week 18	25

Week 1 indicates starting week of Semester.
Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments.

Semester III

Title of the Course and Course Code:	**L**	**T**	**P**	**Cr**
Dissertation Phase I 3EN690	0	0	8	4

Course Objectives :

1. To identify the domain of research
2. To recognize the various means of technical publications and terminologies associated with publications
3. To categorize the research material related to the domain of choice
4. To formulate and articulate research problem with the help of the guide elaborating the research.
5. To obtain information independently and assessing its relevance for answering the research questions

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive Level	Bloom's Cognitive Descriptor
CO1	Conduct in-depth literature survey confined to the domain of dissertation work	Analyzing	Identify, Examine
CO2	Develop presentation skills to deliver the technical contents obtained through literature survey	Creating	Produce, Create
CO3	Prepare Synopsis/ Outline of dissertation work	Creating	Develop, Organize, Prepare
CO4	Analyze the findings and work of various authors in the area of the dissertation work	Analyzing	Analyze,

CO-PO Mapping :

PO	1	2	3	4	5	6
CO1	3					
CO2		3				
CO3		2				
CO4				2		
3-H, 2-M, 1-L						

Lab Assessment:

There are four components of lab assessment, LA1, LA2, LA3 and Lab ESE.
IMP: Lab ESE is a separate head of passing.

Assessment	Based on	Conducted by	Conduction and Marks Submission	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 4 Submission at the end of Week 5	25
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 5 to Week 8 Submission at the end of Week 9	25
LA3	Lab activities, attendance, journal	Lab Course Faculty	During Week 10 to Week 14 Submission at the end of Week 14	25
Lab ESE	Lab Performance and related documentation	Lab Course faculty	During Week 15 to Week 18 Submission at the end of Week 18	25

Week 1 indicates starting week of Semester.
Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course.

Title of the Course and Course Code:	L	T	P	Cr
Dissertation Phase II 3EN691, 3EN692	0	0	12	6

Course Objectives :

1. To follow methodology precisely and meet the objectives of proposed work
2. To test rigorously before deployment of system
3. To validate the work undertaken

4. To consolidate the work as furnished report

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive	
		Level	**Descriptor**
CO1	Demonstration evidence of independent investigation	Understanding	Explain
CO2	Critically analyze the results and their interpretation; infer findings	Analyzing	Compare, Classify
CO3	Prepare a report and present the original results in an systematic way	Creating	Write, Compose
CO4	Interpret practical inferences and limitations of the subject that he/ she has chosen for dissertation work	Understanding	Summarize

CO-PO Mapping :

PO	**1**	**2**	**3**	**4**	**5**	**6**
CO1	3					
CO2		3				
CO3		2				
CO4				2		
3-H, 2-M, 1-L						

Lab Assessment:

There are four components of lab assessment, LA1, LA2, LA3 and Lab ESE.
IMP: Lab ESE is a separate head of passing.

Assessment	Based on	Conducted by	Conduction and Marks Submission	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 4 Submission at the end of Week 5	25
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 5 to Week 8 Submission at the end of Week 9	25
LA3	Lab activities, attendance, journal	Lab Course Faculty	During Week 10 to Week 14 Submission at the end of Week 14	25
Lab ESE	Lab Performance and related documentation	Lab Course faculty	During Week 15 to Week 18 Submission at the end of Week 18	25

Week 1 indicates starting week of Semester.
Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course.

Course Contents:

In Dissertation Phase–II, the student shall consolidate and complete the remaining part of the dissertation work in the field of Electronics Engineering which will consist of implementation of devised algorithm/ system using simulation tool and/or selected hardware, testing, results, measuring performance, comparative analysis, validation of results and conclusions.

The student shall prepare the duly certified final report of Dissertation in standard format for satisfactory completion of the work by the concerned guide and head of the Department.

The students are expected to validate their study undertaken by publishing it at standard platforms. The investigations and findings need to be validated appropriately at standard platforms – conference and/or peer reviewed journal.

The student will be assessed by a panel of examiners in the department for ISE 1 and ISE 2. In ESE there will be one external examiner, internal examiner/guide and a chairman for assessment. The assessment will be broadly based on literature study, work undergone, content delivery, presentation skills, documentation and report.

Title of the Course and Course Code: Professional Elective 5 **Artificial Intelligence 3EN611**	**L**	**T**	**P**	**Cr**
	3	0	0	3

Pre-Requisite Courses: Programming Knowledge

Textbooks:

1. Mariusz Flasiński, Introduction to Artificial Intelligence, Springer, 1st edition, 2016
2. Stuart Russell and Peter Norvig, Artificial Intelligence – A Modern Approach, Prentice Hall Series, Third Edition 2010
3. Michael Negnevitsky, Artificial Intelligence- A guide to intelligent systems, Pearson Education, second edition, 2005

References:

1. N J Nilsson,Morgan, Principles of Artificial Intelligence, Kaufmann Publishers Inc. San Francisco, CA, USA, 1980

2. Elaine Rich, Kevin Knight, Shivashankar B Nair, Artificial Intelligenc, , Tata McGraw Hill Publishing Company Limited, Third edition 2009

Course Objectives :

1. To introduce foundation of Artificial Intelligence and Neural network
2. To introduce knowledge of Expert systems, artificial neural networks, fuzzy systems and evolutionary computation technologies
3. To articulate logic of various Search methods, Heuristic Search methods, Pattern recognition and cluster analysis
4. To introduce tools supporting these technologies

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	**Bloom's Cognitive**

		Level	Descriptor
CO1	Articulate principles behind intelligent systems, knowledge of Expert systems, artificial neural networks, fuzzy systems and evolutionary computation etc.	Understanding	Describe
CO2	Implement Search algorithms, Pattern recognition and cluster analysis	Applying	Demonstrate
CO3	Develop small rule-based and frame-based expert systems, explore artificial neural networks, and implement a simple problem as a genetic algorithm.	Analysing	Construct
CO4	Use of MATLAB Neural Network Toolbox	Applying	Execute

CO-PO Mapping :

PO	**1**	**2**	**3**	**4**	**5**	**6**
CO1			2			
CO2				2		
CO3	2					
CO4				1		
3-H, 2-M, 1-L						

Assessment:

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weightage respectively.

Assessment	Marks
ISE 1	10
MSE	30
ISE 2	10
ESE	50

ISE 1 and ISE 2 are based on assignment, oral, seminar, test (surprise/declared/quiz), and group discussion.[One assessment tool per ISE. The assessment tool used for ISE 1 shall not be used for ISE 2]

MSE: Assessment is based on 50% of course content (Normally first three modules)

ESE: Assessment is based on 100% course content with70-80% weightage for course content (normally last three modules) covered after MSE.

Course Contents:

Module 1	**Hrs.**
Introduction: What is AI, Foundation of artificial intelligence, history of artificial intelligence, Symbolic Artificial Intelligence, Computational Intelligence	**6**
Module 2	**Hrs.**
Expert Systems: Rule based expert systems, Fuzzy expert systems, Frame based expert systems	**7**
Module 3	**Hrs.**
Search Methods: State Space and Search Tree, Blind Search, Heuristic Search, Adversarial Search, Search for Constraint Satisfaction Problems, Special Methods of Heuristic Search.	**7**
Module 4	**Hrs.**
Evolutionary computing: Simulation of natural evolution, Genetic Algorithms, Evolution Strategies, Evolutionary Programming, Genetic Programming, Other Biology-Inspired Models	**6**
Module 5	**Hrs.**

Pattern Recognition and Cluster Analysis, Problem of Pattern Recognition, Minimum Distance Classifier, Nearest Neighbor Method, Decision-Boundary-Based Classifiers, Statistical Pattern Recognition, Decision Tree Classifier, Cluster Analysis	**7**
Module 6	**Hrs.**
Artificial Neural Networks: Introduction, how the brain works ,The neuron as a simple computing element, The perceptron, Multilayer neural networks, Accelerated learning in multilayer neural networks, The Hopfield network, Bidirectional associative memory, Self-organising neural networks	**7**

Module wise Measurable Students Learning Outcomes :

Module 1: Describe principles behind intelligent systems, knowledge of artificial neural networks.
Module 2: Develop small rule-based expert systems and implement a simple problem as a genetic algorithm.
Module 3: Implement Search algorithms such as Blind Search, Heuristic Search, Adversarial Search etc.
Module 4: Catch knowledge of evolutionary computation
Module 5: Implement Pattern recognition and cluster analysis
Module 6: Explore artificial neural networks and implement a simple problem using various learning rules

Title of the Course and Course Code: Professional Elective 5	**L**	**T**	**P**	**Cr**
Automotive Electronics 3EN612	3	0	0	3

Pre-Requisite Courses:

Textbooks:

1. **Bosch Automotive Electrics and Automotive Electronics by Robert Bosch**

4. **References:** https://elearning.vector.com/vl_can_introduction_en.html
5. https://www.nxp.com/docs/en/reference-manual/BCANPSV2.pdf
6. http://www.analog.com/media/en/technical-documentation/application-notes/AN-1123.pdf
7. https://www.autosar.org/
8. https://elearning.vector.com/vl_autosar_introduction_en.html
9. https://www.kpit.com/resources/downloads/kpit-autosar-handbook.pdf
10. https://www.autosar.org/fileadmin/user_upload/standards/classic/3-2/AUTOSAR_Glossary.pdf
11. https://www.autosar.org/fileadmin/user_upload/standards/classic/3-2/AUTOSAR_LayeredSoftwareArchitecture.pdf
12. https://www.autosar.org/fileadmin/user_upload/standards/classic/3-0/AUTOSAR_TechnicalOverview.pdf

Course Objectives :

1. Overview of Automotive electronics system and its components.
2. Automotive sensor and actuator software modules.
3. CAN J1939 protocol
4. AUTOSAR technical overview

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive	
		Level	Descript
CO1	Illustrate significance of AUTOMOTIVE Electronics	Understanding	Illustrate
CO2	Develop automotive subsystems, Interfaces for automotive sensors and actuators software modules as closed loop	Applying	Develop
CO3	Develop Communication between various controllers using CAN bus and others buses	Applying	Develop
CO4	Explain the AUTOSAR layered architecture	Understanding	Explain
CO5	Develop Model based automotive system using MATLAB	Creating	Develop
CO6	Illustrate automotive systems for EMC complaint	Understanding	Illustrate

CO-PO Mapping :

PO	1	2	3	4	5	6
CO1			2			
CO2				2		
CO3			2			
CO4				1		

CO5			1			
CO6				2		
3-H, 2-M, 1-L						

Assessment:

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weightage respectively.

Assessment	Marks
ISE 1	10
MSE	30
ISE 2	10
ESE	50

ISE 1 and ISE 2 are based on assignment, oral, seminar, test (surprise/declared/quiz), and group discussion.[One assessment tool per ISE. The assessment tool used for ISE 1 shall not be used for ISE 2]
MSE: Assessment is based on 50% of course content (Normally first three modules)
ESE: Assessment is based on 100% course content with70-80% weightage for course content (normally last three modules) covered after MSE.

Course Contents:

Module 1 : Overview of Automotive electronics system and its components	**4**
Automotive Market: On road vehicle, off road vehicle, safety and connectivity Hardware :ECU-ICs, PCB, Sensors, Actuators Software: Boot Loader, OS + Application, Calibration parameters. Battery charging system, Engine control system, Steering control system, Automatic transmission system, Cruise control system.	
Module 2: Automotive sensor and actuator software modules	**8**
Sensor: Temperature, Air Mass sensor, Pressure sensor, Speed sensors, Knocking Sensor, Lamda (Oxygen) Sensor, Throttle Position sensor, Cam sensor, Crank position sensor. Physical Sensor Connection, Sensor environment, Harness, Reference voltage, closed loop sensor software module, Calibration, OORH, OORL, In Range, Auto and Manual mode. Actuator: Physical actuator, Actuator driver faults, shorted to Low, Shorted to High, Open circuit. Check to give ON/OFF commands. Failure Mode Identification.	
Module 3 :: Communication protocol	**6**
CAN Bus, CAN J1939 Protocol, LIN Bus ,Flex ray, Automotive Ethernet, RF, Bluetooth, WiFi, Diagnostic Protocol: UDS, Inter-ECU communication protocol, Inter vehicle communication to form autonomous vehicle system Tools: CANoe, Vehicle spy, CAPEL,TAE scripting	
Module 4: Software Architecture	**6**
Classical architecture, Layered architecture (AUTOSAR), Increased E/E complexity, AUTOSAR organization, All layer information(e.g. RTE,BSW, applications) Tools: Davinci developer, configurator, Raphsody	
Module 5: Model based Development:	**8**
Algorithm/application development using Simulink, Stateflow, Code generation for various control algorithms like ESP,ABS, TCS etc.	

Module 6: Electromagnetic Compatibility	4
Introduction to various regulatory requirements and international electrical and EMC standards, Understanding origin of pulses, disturbances, circuit and PCB layout design techniques to meet EMC.	

Module wise Measurable Students Learning Outcomes : student will

Module 1: describe "AUTOMOTIVE Electronics system"

Module 2: Develop automotive subsystems and Interfaces for automotive sensors and actuators

Module 3: Develop Communication between various controllers

Module 4: Explain the AUTOSAR layered architecture in automotive electronics

Module 5: Develop Model based automotive system using MATLAB

Module 6: Explain EMC compliance of automotive systems

Title of the Course and Course Code: **Professional Elective 5**

Introduction to Machine Learning 3EN613

L	T	P	Cr
3	0	0	3

Pre-Requisite Courses: probability & statistics

Textbooks:

1. Tom Mitchell, "Machine Learning" First Edition, McGraw- Hill, 1997.
2. Ethem Alpaydin, "Introduction to machine learning", 2nd edition, The MIT Press

References:

1. Alex Smola and S.V.N. Vishwanathan, "Introduction to Machine Learning", Cambridge University Press 2008.
2. Christopher Bishop, "Pattern Recognition and Machine Learning", Springer, 2006.

Course Objectives :

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive level	Descriptor
CO1	Apply knowledge of computing and mathematics to machine learning problems, models and algorithms	Applying	Apply
CO2	Analyse a problem and identify the computing requirements appropriate for its solution	Analyzing	Analyse
CO3	Design, implement, and evaluate an algorithm to meet desired needs	creating	Design

CO-PO Mapping :

PO	1	2	3	4	5	6
CO1			2			
CO2				2		
CO3	2					
3-H, 2-M, 1-L						

Assessments :

Teacher Assessment:

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weights respectively.

Assessment	Marks
ISE 1	10
MSE	30
ISE 2	10
ESE	50

ISE 1 and ISE 2 are based on assignment/declared test/quiz/seminar etc.
MSE: Assessment is based on 50% of course content (Normally first three modules)
ESE: Assessment is based on 100% course content with 70-80% weightage for course content (normally last three modules) covered after MSE.

Course Contents:

Module 1: Machine Learning	**Hrs.**
Introduction, Supervised Learning, Learning a Class from Examples, Learning Multiple Classes, Regression, Dimensions of a Supervised Machine Learning Algorithm, Bayesian Decision Theory, Discriminant Functions, Association Rules	**6**
Module 2: Parametric, Multivariate and Nonparametric Methods	**Hrs.**
Maximum Likelihood Estimation, Evaluating an Estimator: Bias and Variance, The Bayes' Estimator, Parametric Classification, Multivariate Data, Multivariate Normal Distribution, Multivariate Classification, Multivariate Regression, Nonparametric Density Estimation, Nonparametric Classification, Nonparametric Regression: Smoothing Models	**6**
Module 3 Dimensionality Reduction**,** Clustering and Decision Trees	**Hrs.**
Principal Components Analysis, Factor Analysis, Linear Discriminant Analysis, Locally Linear Embedding, Mixture Densities, k-Means Clustering, Expectation-Maximization Algorithm, Supervised Learning after Clustering, Hierarchical Clustering, Univariate Trees, Rule Extraction from Trees, Learning Rules from Data, Multivariate Trees	**8**
Module 4 Linear Discrimination and Multilayer Perceptrons	**Hrs.**
Generalizing the Linear Model, Geometry of the Linear Discriminant, Parametric Discrimination Revisited, Gradient Descent, Logistic Discrimination, Discrimination by	**6**

Regression, The Perceptron, Training a Perceptron, Learning Boolean Functions, Multilayer Perceptrons, Backpropagation Algorithm, Training Procedures, Bayesian View of Learning, Dimensionality Reduction, Learning Time	
Module 5 Kernel Machines and Bayesian Estimation	**Hrs.**
Optimal Separating Hyperplane, The Nonseparable Case: Soft Margin Hyperplane, ν-SVM, Kernel Trick, Vectorial Kernels, Multiple Kernel Learning, Multiclass Kernel Machines, Kernel Machines for Regression, Estimating the Parameter of a Distribution, Bayesian Estimation of the Parameters of a Function, Gaussian Processes	**6**
Module 6 Hidden Markov Models and Graphical Models	**Hrs.**
Discrete Markov Processes, Hidden Markov Models, Three Basic Problems of HMMs, Evaluation Problem, Finding the State Sequence, Learning Model Parameters, Model Selection in HMM, Canonical Cases for Conditional Independence, Example Graphical Models, d-Separation, Belief Propagation, Undirected Graphs: Markov Random Fields, Learning the Structure of a Graphical Model, Influence Diagrams	**8**

Module wise Measurable Students Learning Outcomes :

After the completion of the course the student should be able to:

Module 1: Relate the basic concepts and methods of machine learning.

Module 2: Classify estimation technique

Module 3: Contrast classification using clustering technique

Module 4: Choose training and back propagation algorithm for classification

Module 5: Distinguish kernel machines for regression

Module 6: Evaluate Hidden Markov model for learning and classification

Title of the Course and Course Code: Professional Elective 5	**L**	**T**	**P**	**Cr**
DSP Architecture 3EN614	3	0	0	3

Pre-Requisite Courses: Digital signal processing

Textbooks:

1. Rohit Chandra, Ramesh Menon, Leo Dagum, David Kohr, DrorMaydan, Jeff McDonald,"Parallel Programming in OpenMP", 1st Edition, Morgan Kaufman,2000.
2. Ann Melnichuk,Long Talk, "Multicore Embedded systems", 1st Edition, CRC Press,2010.
3. Wayne Wolf, "High Performance Embedded Computing: Architectures, Applications and Methodologies", 1st Edition, Morgan Kaufman, 2006.

References:

1. M. Sasikumar, D. Shikhare, Ravi Prakash, "Introduction to Parallel Processing", 1st Edition, PHI, 2006.
2. Fayez Gebali, "Algorithms and Parallel Computing",1st Edition, John Wiley & Sons, 2011
3. E.S.Gopi, "Algorithmic Collections for Digital Signal Processing Applications Using MATLAB", 1st Edition, Springer Netherlands,2007.
4. Website ti.com

Course Objectives :

1. Identify and formalize architectural level characterization of P-DSP hardware
2. Ability to design, programming (assembly and C), and testing code using Code Composer Studio environment
3. Deployment of DSP hardware for Control, Audio and Video Signal processing applications
4. Understanding of major areas and challenges in DSP based embedded systems

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	**Bloom's Cognitive**	
		Level	**Descripto**
CO1	Illustrate the DSP hardware architecture	Illustrating	Illustrate
CO2	Illustrate Multicore DSP processors	Illustrating	Illustrate
CO3	Develop applications using assembly and C with DSP processors	Creating	Develop
CO4	Develop FPGA based DSP systems	Creating	Develop
CO5	Create High Performance Computing systems using P-DSP	Illustrating	Illustrate

CO-PO Mapping :

PO	**1**	**2**	**3**	**4**	**5**	**6**
CO1			2			
CO2				2		
CO3	2					
CO4	1					
CO5			2			
3-H, 2-M, 1-L						

Assessment:

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weightage respectively.

Assessment	Marks
ISE 1	10
MSE	30
ISE 2	10
ESE	50

ISE 1 and ISE 2 are based on assignment, oral, seminar, test (surprise/declared/quiz), and group discussion.[One assessment tool per ISE. The assessment tool used for ISE 1 shall not be used for ISE 2]

MSE: Assessment is based on 50% of course content (Normally first three modules)

ESE: Assessment is based on 100% course content with70-80% weightage for course content (normally last three modules) covered after MSE.

Course Contents:

Module 1 : Programmable DSP Hardware	**4**
Processing Architectures (von Neumann, Harvard), DSP core algorithms (FIR, IIR, Convolution, Correlation, FFT), IEEE standard for Fixed and Floating Point Computations, Special Architectures Modules used in Digital Signal Processors (like MAC unit, Barrel shifters), On-Chip peripherals, DSP benchmarking.	
Module 2: Structural and Architectural Considerations	**8**
Parallelism in DSP processing, Texas Instruments TMS320 Digital Signal Processor Families, Fixed Point TI DSP Processors: TMS320C5414 Family, Internal Architecture, Arithmetic and Logic Unit, Auxiliary Registers, Addressing Modes (Immediate, Direct and Indirect, Bit-reverse Addressing), Basics of TMS320C55XX DSP Architecture, Memory Map, Interrupt System, Peripheral Devices, Illustrative Examples for assembly coding.	
Module 3 : VLIW Architecture:	**6**
Current DSP Architectures, GPUs as an alternative to DSP Processors, TMS320C6X Family, Addressing Modes, Replacement of MAC unit by ILP, Detailed study of ISA, Assembly Language Programming, Code Composer Studio, Mixed C and Assembly Language programming, On-chip peripherals, Simple applications developments as an embedded environment.	
Module 4: Multi-core DSPs:	**6**
Introduction to Multi-core computing and applicability for DSP hardware, Concept of threads, introduction to P-thread, mutex and similar concepts, heterogeneous and homogenous multi-core systems, Shared Memory parallel programming – OpenMP approach of parallel programming, PRAGMA directives, OpenMP Constructs for work sharing like for loop, Sections, TI TMS320C6678 (Eight Core subsystem).	
Module 5: FPGA based DSP Systems	**8**
Limitations of P-DSPs, Requirements of Signal processing for Cognitive Radio (SDR), FPGA based signal processing design-case study of a complete design of DSP processor.	
Module 6: High Performance Computing using P-DSP:	**4**
Preliminaries of HPC, MPI, OpenMP, multicore DSP as HPC infrastructure.	

Module wise Measurable Students Learning Outcomes : student will

Module 1: Illustrate DSP processor architecture

Module 2: : Develop DSP programming

Module 3: Develop programs using VLIW Architecture CPU

Module 4: Illustrate multicore DSP CPUs

Module 5: Design FPGA based DSP system Module 6: Illustrate High Performance Computing using P-DSP

Semester IV

Sr.No.	Category	Course Code	Course Name
1	PC	3ST693	Dissertation Phase-III
2	PC	3ST694	Dissertation Phase-IV
3	PC	3ST695	Dissertation Phase-IV
5	MC	3IC6**	Mandatory Non Credit Course