Walchand College of Engineering, Sangli

(Government Aided Autonomous Institute)

Course Contents (Syllabus) for

First Year M. Tech
(Electronics Engineering)
Sem. I to II

AY 2020-21

Semester I

Title of the Course and Course Code:	L	T	P	Cr
Research Methodology for Electronics Engineers 4IC501	2	0	0	2

Pre-Requisite Courses: Electronics Engineering

Textbooks:

1. C. R. Kothari, Research Methodology Methods and Techniques, New Age international, 2nd Edition, 2009
2. Deepak Chopra and Neena Sondhi, *Research Methodology : Concepts and cases,* Vikas Publishing House, New Delhi, 2008

References:

1. E. Philip and Derek Pugh, How to get a Ph. D. – a handbook for students and their supervisors, Open university press,5th Edition,2010
2. Stuart Melville and Wayne Goddard, Research Methodology: An Introduction for Science & Engineering Students, Kenwyn, South Africa : Juta & Co. Ltd., 1996.

Course Objectives :

1. To develop a research orientation among the students and to acquaint them with fundamentals of research methods
2. To develop understanding of the basic framework of research process and techniques.
3. To identify various sources of information for literature review and data collection.
4. To develop an understanding of the ethical dimensions of conducting applied research.
5. Appreciate the components of scholarly writing.

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive Level	Descriptor
CO1	Identify/formulate research the problem for M. Tech. dissertation	Remembering	Describe
CO2	Articulate a review paper in the format of standard Journal/transactions by reviewing at least 10 papers (from standard Journals /transactions /Reference Books/Handbooks etc) related to a	Understanding	Explain
CO3	To deliver a seminar on the same, prepare a presentation giving critical analysis of the subject and possible outcomes	Evaluating	Discuss
CO4	Write dissertation/thesis after completion of the work for the degrees of M. Tech.	Creating	Compose

CO-PO Mapping :

PO	1	2	3	4	5	6
CO1	**2**					
CO2		**2**				
CO3		**2**				
CO4				1		
3-H, 2-M, 1-L						

Assessment:

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weightage respectively.

Assessment	Marks
ISE 1	10
MSE	30
ISE 2	10
ESE	50

ISE 1 and ISE 2 are based on assignment, oral, seminar, test (surprise/declared/quiz), and group discussion.[One assessment tool per ISE. The assessment tool used for ISE 1 shall not be used for ISE 2]

MSE: Assessment is based on 50% of course content (Normally first three modules)

ESE: Assessment is based on 100% course content with70-80% weightage for course content (normally last three modules) covered after MSE.

Course Contents:

Module 1	**Hr**
Introduction Concepts of Research, Meaning and Objectives of Research, Research Process, Types of Research, Criteria of Good Research, Research Problem – Identifying and Defining, Research Proposals – Types, contents, Sponsoring agency's requirements, Ethical aspects, IPR issues like patenting, copyrights	**4**
Module 2	**Hr**
Research Design Meaning, Need and Types of research design, Literature Survey and Review, Research Design Process, Measurement and scaling techniques, Data Collection – concept, types and methods, Processing and analysis of data, Quantitative Techniques Sampling fundamentals, Design of Experiments.	**4**
Module 3	**Hr**
Quantitative Techniques Sampling fundamentals, Testing of hypothesis using various tests like Multivariate analysis, Use of standard statistical software, Data processing, Preliminary data analysis and interpretation, Uni-variate and bi-variate analysis of data, testing of hypotheses, techniques such as ANOVA, Chi square test etc., Nonparametric tests. Correlation and regression analysis	**5**
Module 4	**Hr**
Measurements based research methods in Signal and Image Processing, Graphics, Vision and Pattern Recognition, , Induction Vs Deduction, Deductive and Inductive Methods in Signal and Image Processing, Graphics, Vision and Pattern, Recognition; Hypothetical-Deductive Method, Repetitions, Patterns, Identity, Causality And Determinism, Godel's Theorem, Fuzzy Logic, Research in the area of VLSI	**5**
Module 5	**Hr**
Research Communication, Writing a conference paper, Journal Paper, Technical report, dissertation/thesis writing. Presentation techniques, Patents and other IPRs, software used for report writing such as WORD, Latex etc.	**5**
Module 6	**Hr**
Case studies: Related to Electronics Engineering.	**3**

Module wise Measurable Students Learning Outcomes :

Module 1: Describe a range of quantitative and qualitative research designs

Module 2: Identify the advantages and disadvantages associated with research designs

Module 3: Explain the testing of hypothesis

Module 4: Recognize the keys in Electronics Engineering research

Module 5: Write and present review paper in conference or in journal

Module 6: Design an appropriate mixed-method research study to solve a problem in the field of Electronics Engineering

Title of the Course and Course Code: Advanced Digital Signal Processing 4EN501	L	T	P	Cr
	3	0	0	3

Pre-Requisite Courses: Signals and Systems, Digital Signal Processing

Textbooks:

1. Sanjit K. Mitra, "Digital Signal Processing – A Computer based approach", Tata McGraw-Hill, 4th Edition , 2013
2. Bernard Widrow, Samuel D. Stearns "Adaptive Signal Processing,", Prentice-Hall, Englewood Cli, NJ, 1985

References:

1. J. G. Proakis, Dimitris K Manolakis, "Advanced Digital Signal Processing Principals, Algorithms and Applications,", Pearson,2007

Course Objectives :

1. To illustrate the concepts of Advanced Signal Processing.
2. To explain the different techniques for design of filters and multirate systems.
3. To enable the students for the design and development of Adaptive DSP systems.

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive	
		Level	**Descriptor**
CO1	Explain the basic and advanced signal processing concepts.	Understanding	Discuss
CO2	Design FIR and IIR filters with given specifications.	Creating, Applying	Design, Solve
CO3	Analyse the various algorithms related with multi-rate DSP	Analysing	Explain
CO4	Illustrate adaptive signal processing algorithms	Applying	Demonstrate

CO-PO Mapping :

PO	1	2	3	4	5	6
CO1			2			
CO2						1
CO3				2		
CO4			1			
3-H, 2-M, 1-L						

Assessment:

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weightage respectively.

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ISE 1	10
MSE	30
ISE 2	10
ESE	50

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MSE: Assessment is based on 50% of course content (Normally first three modules)
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Course Contents:

1	**Module 1: Review of Digital Signal Processing**	**Hrs**
	Discrete Time Signals and systems, LTI Systems, Basic Signal Processing Operations, Discrete Time Systems-Classification, impulse and step responses, phase and group delays. Time domain and frequency domain characterization of LTI discrete time systems, Z Transform, Transfer function	**8**
2	**Module 2: DSP Structures**	**Hrs**
	Block Diagram Representation, Equivalent Structures, Basic FIR Digital Filter Structures, Basic IIR Digital Filter Structures, All pass Filters, Tuneable IIR Digital Filters, IIR Tapped Cascaded Lattice Structures, FIR Cascaded Lattice Structures, Parallel All pass Realization of IIR Transfer Functions	**6**
3	**Module 3: DFT Computation Techniques**	**Hrs**
	DFT-Definition and properties, symmetry properties, Circular convolution, Computation of DFT, Decimation in time (DIT) and Decimation in Frequency (DIF) Fast Fourier transform (FFT) algorithms , Linear filtering using FFT- overlap add, overlap save methods, Goertzel Algorithm	**6**
4	**Module 4: Filter Design Techniques**	**Hrs**
	Bilinear Transformation Method of IIR Filter Design, Design of Low pass IIR Digital Filters, Design of High pass, Band pass and Band stop IIR Digital Filters, Spectral Transformations of IIR Filters, FIR Filter Design Based on Windowed series, Design of Digital Filters with Least-Mean-Square Error, Constrained Least-Square Design of FIR Digital Filters	**8**
5	**Module5: Multi-rate Signal Processing**	**Hrs**
	The Basic Sample Rate Alteration Devices, Filters in Sampling Rate Alteration Systems, Multistage Design of Decimator and Interpolator, The Poly phase Decomposition, Arbitrary-Rate Sampling Rate Converter, Digital Filters Banks, Two-Channel Quadrature-Mirror Filter bank	**6**
6	**Module 6: Introduction to adaptive signal processing**	**Hrs**
	Introduction to Adaptive Filters, Steepest descent technique, LMS algorithm-Convergence analysis, Learning curve, SVD.	**6**

Module wise Measurable Students Learning Outcomes :

Module 1: Discuss the Digital Signal Processing concepts
Module 2 : Explain and construct the DSP structures
Module 3 : Solve the problems using DFT algorithms
Module 4 : Design FIR and IIR filter
Module 5 : Explain multi rate signal processing
Module 6 : Demonstrate adaptive signal processing algorithms

Tutorial: Tutorial will be engaged in either of following

1. Solving numerical
2. Writing and executing MATLAB programs for various algorithms in ADSP

Title of the Course and Course Code:	L	T	P	Cr
Embedded System Design 4EN502	3	0	0	3

Pre-Requisite Courses: Microprocessors / Microcontrollers

Textbooks:

1. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2nd Edition
2. Frank Vahid and Tony Givargis, "Embedded System Design", Wiley

References:

1. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing", Morgan Kaufman Publication
2. Steve furber, "ARM System-on-Chip Architecture", Pearson Education
3. Frank Vahid and Tony Givargis, "Embedded System Design", Wiley
4. Technical references and user manuals on www.arm.com, NXP Semiconductor www.nxp.com and Texas Instruments www.ti.com, ST Microelectronics www.st.com.

Course Objectives : At the end of this course, students will be able to

1. Understand ARM processor core architecture with several features of peripherals available on various embedded Cortex- M processors.
2. Understand interrupts and its programming with peripherals
3. Develop small embedded system by using the ARM processor core based systems and application software for it.
4. Use EDA tools to design embedded system PCB.
5. Interface various memories with cortex M processor.

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive Level	Descript
CO1	Illustrate Cortex M processor architecture and its features	Understanding	Illustrate
CO2	Develop programs for peripherals and interrupts	Applying	Develop
CO3	Designing embedded system hardware	Creating	Design
CO4	Design embedded system software.	Creating	Design
CO5	Design Interface for various memories with Embedded system	Creating	Design

CO-PO Mapping :

PO	1	2	3	4	5	6
CO1			2			
CO2				2		
CO3			2			
CO4				1		
3-H, 2-M, 1-L						

Assessment:

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weightage respectively.

Assessment	Marks
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MSE	30
ISE 2	10
ESE	50

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MSE: Assessment is based on 50% of course content (Normally first three modules)
ESE: Assessment is based on 100% course content with70-80% weightage for course content (normally last three modules) covered after MSE.

Course Contents:

Module 1: ARM Cortex –M Architecture and Programming:	**6**
ARM Cortex M3/M4 Architecture, Registers, CPU status, Clock generation, Memory organization, Instruction Set, Programming model – Registers, Operation Modes, Embedded C Programming	
Module 2: Cortex M CPU Interrupts	**6**
Nested Vectored Interrupt Controller (NVIC), Vector table, Interrupt priorities, Interrupt Inputs and Pending behavior, Fault Exceptions, Supervisor and Pendable Service Call, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency, Startup files, initialization of peripherals interrupts, Interrupt routines programming.	
Module 3 : ARM Peripherals and Programming	**8**
On chip peripherals, GPIO, RTC, Watchdog, UART, I2C, I2S, ADC and SPI interfacing and Programming, Repetitive interrupt timer, PWM Block programming, CAN BUS programming, LIN bus programming, DMA programming,Writing LCD drives, Drivers for serial port communication	
Module 4: Embedded System Design and Testing	**8**
Design embedded system using Cortex-M3/M4 processors with SPI, UART, ADC, DAC, Memory, PWM peripherals. Hardware design issues, State Machine based Embedded Programming, Writing initialisation programs, Debugging techniques, Debugging with JTAG, Debugging with UART port.	
Module 5 : Memory	**6**
Types of Memory, static, dynamic, SDRAM, DDR RAM, Flash Memory chips, SD Card, Quad SPI Flash Interface with CPU.	
Module 6 : Hardware design issues	**6**
Selection of electronics components, Reading Schematic, Datasheets, footprints of various components, EDA tool for PCB design, Hierarchical design, Schematic and board layout design,	

board assembly process, board bring-up, cold and hot testing	

Module wise Measurable Students Learning Outcomes : student will able to

Module 1: Illustrate Cortex-M embedded CPU programming model

Module 2: Illustrate Cortex-M CPU interrupts and develop programs using interrupts

Module 3: Develop peripheral programming

Module 4: Design embedded system with peripherals

Module 5: Design embedded system with various memories

Module 6: Design schematic, PCB layout with EDA Tools and test it.

Title of the Course and Course Code:	**L**	**T**	**P**	**Cr**
Electronics Lab 1 4EN551	0	0	4	2

Pre-Requisite Courses: Microprocessors / Microcontrollers

Textbooks:

1. Joseph Yiu, “The definitive guide to ARM Cortex-M3”, Elsevier, 2nd Edition
2. Frank Vahid and Tony Givargis, “Embedded System Design”, Wiley
3. User and reference guide of LPC1768
4. Philips- An Indroduction to SDRAM and memory controller by Benny Akesson
5. Rigid Flex PCB design – by Ben Jordan

References:

1. Sloss Andrew N, Symes Dominic, Wright Chris, “ARM System Developer's Guide: Designing and Optimizing”, Morgan Kaufman Publication
2. Steve furber, “ARM System-on-Chip Architecture”, Pearson Education
3. Technical references and user manuals on www.arm.com, NXP Semiconductor www.nxp.com and Texas Instruments www.ti.com, ST Microelectronics www.st.com.

4. www.altium.com

Course Objectives : At the end of this course, students will be able to

1. Understand ARM processor core architecture with several features of peripherals available on LPC1768 embedded Cortex- M processors.
2. Understand interrupts and its programming with peripherals
3. Develop small embedded system by using the ARM processor core based systems and application software for it.
4. Use EDA tools to design embedded system PCB.
5. Interface various memories with cortex M processor.

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive Level	Descript
CO1	Illustrate Cortex M processor architecture and its features	Understanding	Illustrate
CO2	Develop and execute programs for peripherals and interrupts	Applying	Develop
CO3	Design and execute embedded system software	Creating	Design
CO4	Design embedded system PCB	Creating	Design

CO-PO Mapping :

PO	1	2	3	4	5	6
CO1			2			
CO2				2		
CO3			2			
CO4				1		
3-H, 2-M, 1-L						

Lab Assessment:

There are four components of lab assessment, LA1, LA2, LA3 and Lab ESE.
IMP: Lab ESE is a separate head of passing.

Assessment	Based on	Conducted by	Conduction and Marks Submission	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 4 Submission at the end of Week 5	25
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 5 to Week 8 Submission at the end of Week 9	25
LA3	Lab activities, attendance, journal	Lab Course Faculty	During Week 10 to Week 14 Submission at the end of Week 14	25
Lab ESE	Lab Performance and related documentation	Lab Course faculty	During Week 15 to Week 18 Submission at the end of Week 18	25

Week 1 indicates starting week of Semester.
Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments.

Course Contents:

1. Write Simple C Program with header files for array manipulations
2. Write C programs for GPIO and debug programs, see variables and waveforms.
3. Writing programs for UART in polling mode
4. Writing programs for SPI in interrupt mode
5. Writing programs for I2C and ADC etc. in polling mode
6. Writing programs for Interrupt vector table and writing interrupt programs for UART peripherals.
7. Write Programs with CMSIS for UART, SPI etc.
8. Design Embedded system using various peripherals in group of 2 students
9. Design PCB schematic for embedded system using LPC1768
10. Design Layout for schematic generated in Exp. 9

Experiment wise Measurable Students Learning Outcomes : student will able to

Experiment 1: Develop and execute Cortex-M embedded CPU programs for arrays
Experiment 2: Develop and execute Cortex-M CPU GPIO and debug it.
Experiment 3: Develop and execute peripheral UART programming in polling mode
Experiment 4: Develop and execute program for SPI in interrupt mode
Experiment 5: Develop and execute program for I2C and ADC in polling mode
Experiment 6: Develop and execute program for UART peripherals using interrupt
Experiment 7: Develop and execute program with CMSIS for UART, SPI etc
Experiment 8: Develop and execute program for Embedded system using various peripherals
Experiment 9: Design schematic with EDA Tools and test it.
Experiment 10: Design PCB layout with EDA Tools and test it.

Experiments using MATLAB :

1. Generation and analysis of different signals in time and frequency domains.
2. Study and applications of different transforms
3. Design of Digital Filter: IIR, FIR.
4. Design of multi rate signal system

Experiments using DSK 6713 DSP Kit

5. Introduction to DSK 6713 kit and CCS environment
6. Study of input/output, architecture of C6x processor
7. Digital filter design using DSK 6713
8. Implementation of DSP applications using DSK 6713

Title of the Course and Course Code: **Professional Elective I: Digital VLSI Design 4EN511**	**L**	**T**	**P**	**Cr**
	3	0	0	3

Pre-Requisite Courses: Digital Techniques

Textbooks:

1. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "*Digital Integrated Circuits, A System Perspective*", Pearson Education, Second Edition, First Indian Reprint, 2003.
2. Neil Weste, Kamran Eshraghian "*Principles of CMOS VLSI Design*", Addison Wesley/Pearson Education, 2010

References:

1. Kamran Eshraghian, Pucknell and Eshraghian "*Essentials of VLSI Circuits and Systems*", , Prentice-Hall (India), 2008
2. Sung-Mo Kang, Yusuf Leblebici "*CMOS Digital Integrated Circuits: Analysis and Design*", McGraw Hill Education (India), Third Edition, 2003
3. Neil Weste, David Harris, Ayan Banerjee "*CMOS VLSI Design*", Pearson Education, 2008

Course Objectives:

1. To explain the relevance of CMOS technology in implementing digital circuits.
2. To discuss in details various logic styles (static, dynamic) in implementing CMOS circuits and the effect of choosing a particular style on device performance from delay, power and area point of view.
3. To develop the architectures of few data-path designs (system building blocks) and an insight into extracting the functionality of displayed CMOS circuit.
4. To motivate the students to develop lifelong/self-learning attitude.

Course Learning Outcomes:

CO1: Apply the analytical expressions involving physical parameters, process parameters and electrical parameters to characterize the MOS transistors **by taking into account** the fundamental principles involved with MOS devices.

CO2: Analyze static and dynamic CMOS circuits logically to deduct the functionality of the circuits.

CO3: Analyze static and dynamic CMOS circuits numerically to compute the various device parameters and circuit performance parameters.

CO4: Select an appropriate logic style to design submicron MOS transistor based circuits using logical, analytical and computational skills

CO5: **Design** the self timed CMOS circuits, and synchronous circuits with built-in arbiters, synchronizers

CO6: Design with Justification the architectures/schematics of data path design viz adders, multipliers and data shifters.

CO-PO Mapping :

PO	1	2	3	4	5	6
CO1				2		
CO2						1
CO3						1
CO4			2			
CO5			1			
CO6						2
3-H, 2-M, 1-L						

Assessment:

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Assessment	Marks
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MSE	30
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MSE: Assessment is based on 50% of course content (Normally first three modules)

ESE: Assessment is based on 100% course content with70-80% weightage for course content (normally last three modules) covered after MSE.

Course Contents:

Module 1:MOS Transistor	**Hrs.**
MOS transistor theory, MOS under static conditions, Secondary effects, Technology Scaling	**4**
Module 2:CMOS Inverter	**Hrs.**
CMOS inverter, Static and Dynamic behaviour of CMOS inverter, Power and Energy-Delay, Impact of technology scaling on inverter	**6**
Module 3 :Combinational Static Logic Design	**Hrs.**
Combinational static logic designs in CMOS, CMOS (Inverter and Complex gates), pseudo-nmos, pass-transistor logic, transmission gate logic and design aspects for optimizing the performance	**8**
Module 4 :Combinational Dynamic Logic Design	
Combinational dynamic logic designs using pre-charge evaluate logic, domino logic, np-CMOS logic , design aspects for optimizing the performance, Comparison of static and dynamic designs	
Module 5:Sequential Logic Design	**Hrs.**
Timing metrics of sequential circuits, Sequential logic designs in CMOS, Static and dynamic latches and registers	**8**
Module 6:Timing Issues in Digital Circuits	**Hrs.**
Timing Classification, Synchronous Design (Clock skew, Jitter, Clock Distribution), Self-Timed Circuits Design, Synchronizers and arbiters, Using PLL for clock synchronization	**7**

Module wise Measurable Students Learning Outcomes :

Module 1: ALL MOS map to CO1

1. MO1.1: Explain the behaviour of MOS transistor under different biasing conditions
2. MO1.2: Compare between short channel and long channel MOS transistors.
3. MO1.3: Derive the expressions for the equivalent resistance during charging and discharging of the load capacitor.
4. MO1.4: Explain the contribution of various built-in capacitances to the intrinsic load capacitance of the transitor
5. MO1.5: Solve numerical problems based on current-voltage relation under different biasing conditions.

Module 2:

1. MO2.1:Deduct the Voltage Transfer Curve for a CMOS inverter by considering the series combination of pMOS and nMOS transistor and their I-V characteristics in different regions of operation.
2. MO2.2: Derive the analytical expression for switching voltage for CMOS inverter.
3. MO2.3: Explain the piecewise linear model for VTC and derive the expressions for switching threshold (VM), Limiting values of low and high input voltage VIH, VIL, Noise margins corresponding to LOW and HIGH state viz.NMH and MNL
4. MO2.4: Compute the various parasitic capacitances and explain the transient behavior of the inverter in terms of propagation delays.
5. MO2.5: Design the dimensions of NMOS and PMOS transistors of an inverter and chain of inverters to optimize the delay and hence spped.
6. MO2.6: Compute the various components of power dissipation in inverter and optimize the dimensions for optimum energy, power delay and energy delay product.
7. MO2.7: Choose an appropriate low power approach for designing inverters with power

optimization.

Module 3:

1. MO3.1: Design a complementary MOS circuit for a given Boolean function
2. MO3.2: Compute the intrinsic delay by considering the logical and electrical effort and design the dimensions of transistors in the pull-up and pull-down network of the circuit for optimizing the performance.
3. MO3.3: Explain the design techniques for large fan-in combinational circuits.
4. MO3.4: Compute the switching factor and hence dynamic power dissipation for CMOS combinational circuits using probabilistic models.
5. MO3.5: Choose appropriate design approach to reduce switching factor and hence dynamic power dissipation.
6. MO3.6: Develop and design combinational circuits using static styles such as Pseudo-nMOS, Dynamic Switch Cascode Switch Logic (DCVSL), Pass Transistor logic (PL), Complementary Pass Transistor Logic (CPL) and Transmission Gate (TG)Logic.

Module 4:

1. MO4.1: Develop and design combinational circuits using dynamic logic static styles such as Precharge-Evaluate and explain the benefits of this for performance (speed and power) over static logic style.
2. MO4.2: Suggest the solutions to solve the problem of charge leakage, charge sharing, capacitive coupling in dynamic logic circuits.
3. MO4.3: Develop domino CMOS logic and np-CMOS logic, to solve the problem of cascading dynamic logic gates,
4. MO4.4: Select an appropriate CMOS logic style for implementation of CMOS circuits to optimize the performance for speed, area and power.

Module 5:

1. MO5.1: Explain with waveforms the timing metrics of latches and registers.
2. MO5.2: Design static latch and static register using master slave configuration and explain the difference between the two with the help of waveforms
3. MO5.3: Design dynamic latch and dynamic register using pass transistor, transmission gate and solve the problems associated with that logic style.
4. MO5.4: Develop the registers in other logic style viz. C2MOS, Dual Edge Registers, TSPCR etc to improve the performance.
5. MO5.5: Develop the schematics for SR flipflop, Schmitt Trigger, Monostable circuit, Ring Oscillator etc and explain their operation

Module 6:

1. MO6.1: Explain the timing basics of pipelined synchronous circuits and derive the restriction on clock period considering skew and jitter in clock signal.
2. MO6.2: Suggest various clock distribution approaches to minimize the clock skew and jitter problem
3. MO6.3: Develop self timed pipelined circuits by considering the physical and logical ordering of the functional and hand shaking circuit blocks and generating the appropriate hand shake signals.
4. MO6.4: Implement two-phase and four-phase protocol for data communication in self timed circuit

using Muller-C element

5. MO6.5: Design CMOS synchronizers and arbiters for robust operation of synchronous circuits.
6. MO6.6: Compute the reliability figures of CMOS synchronous circuits by taking into considerations the clocking frequency and register related manufacturing parameters.

Title of the Course and Course Code:	L	T	P	Cr
Professional Elective I:Information Theory and Coding 4EN512	3	0	0	3

Pre-Requisite Courses: Probability Theory , Digital Communication

Textbooks:

1. Thomas Cover, Joy Thomas, "*Elements of Information Theory"*, Wiley Publications, second edition.
2. Andre Neabauer, "*Coding Theory: Algorithms, Architectures & Applications*", Wiley Publications, 2010.
3. R Bose, "*Information Theory, Coding and Cryptography*", TMH 2007

References:

1. Simon Haykin*, "Digital Communication"*,Wiley Publications, second edition
2. Jorge Castineira, Moreira,"*Essentials of Error Control Coding*",Wiley, 2006
3. NPTEL lecture series on – "Information theory and coding"

Course Objectives :

1. To discuss in detail about information theory which allows us to analyze and characterize the fundamental limits on communication systems.
2. To explain various approaches of error control coding techniques.

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive Level	Bloom's Cognitive Descriptor
CO1	Analyse performance of channel using information theory.	Analyzing	Integrate
CO2	Illustrate various source coding technique.	Applying	Implement
CO3	Discuss error control coding techniques to improve performance of system.	Evaluating	Estimate

CO – PO Mapping :

PO	1	2	3	4	5	6
CO1	1					
CO2			2			
CO3				2		
3-H, 2-M, 1-L						

Assessment:

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Course Contents:

Module 1 : Review of Probability Theory	**Hrs.**
Random Variable, cumulative distribution function, probability density function, random variable, Bivariate random variable, joint and conditional probabilities.	**5**
Module 2: Entropy, Relative Entropy, and Mutual Information	**Hrs.**
Entropy, Joint Entropy and Conditional Entropy, Relative Entropy and Mutual Information, Measure of Information. Avg. and Mutual Information. Joint and conditional entropy, Rate of Information	**5**
Module 3 : Source Coding and Data Compression	**Hrs.**
Need, Source coding theorem, fixed length coding, variable length coding, kraft Inequality, Huffman Codes, Optimality of Huffman Codes, Shannon- Fanno coding technique, comparative study of source coding technique	**6**
Module 4: Channel Capacity	**Hrs.**
Discrete memoryless source, Symmetric Channels, Properties of Channel Capacity, Jointly Typical Sequences, Channel Coding Theorem, BE-SNR Trade off Fano's Inequality and the Converse to the Coding Theorem, Error Free Communication Over Noisy Channel, Binary Symmetric Channel and Introdution to Continous Sources and Channels	**8**
Module 5 : Linear Binary Block Codes	**Hrs.**
Introduction, Generator and Parity-Check Matrices, Repetition and Single-Parity-Check Codes, Binary Hamming Codes, Error Detection with Linear Block Codes, Weight Distribution and Minimum Hamming Distance of a Linear Block Code, Hard-decision and Soft-decision Decoding of Linear Block Codes, Cyclic Codes, Parameters of BCH and RS Codes, Interleaved and	**8**

Concatenated Codes	
Module 6 : Convolutional Codes	**Hrs.**
Convolutional codes – code tree, trellis, state diagram - Encoding – Decoding: Sequential search and Viterbi algorithm – Principle of Turbo coding	**8**

Module wise Measurable Students Learning Outcomes :

Module 1: Solve numerical on probability theory.

Module 2: Analyse source statistics using fundamentals of information theory

Module 3: Implement different source coding technique.

Module 4: Analyse performance of communication system using channel statistics

Module 5 and 6: Apply error control coding and decoding technique to improve performance of the system.

Title of the Course and Course Code:	**L**	**T**	**P**	**Cr**
Professional Elective 2:Biomedical Signal Processing 4EN515	3	0	0	3

Pre-Requisite Courses: Signals and Systems, Digital Signal Processing

Textbooks:

1. Reddy D C. "*Modern Biomedical Signal Processing – Principles and Techniques*", TMH, New Delhi, 2005
2. Eugene N. Bruce, "*Biomedical Signal Processing and Signal Modeling*", A Wiley-Interscience Publication JOHN WILEY & SONS, INC.

References:

1. Akay M. "*Biomedical Signal Processing*", Academic press, California,1994.
2. Bronzino J D "*The Biomedical Engineering handbook*", CRC and Free press, Florida, 1995.

Course Objectives :

1. To study origins and characteristics of some of the most commonly used biomedical signals including ECG, EEG, evoked potentials, and EMG.
2. To explore application of established engineering methods to complex biomedical signals problems

Course Learning Outcomes:

CO	**After the completion of the course the student should be able to -**	Bloom's Cognitive	
		Level	Descriptor
CO1	Apply signal processing techniques to biomedical signals	3	Applying

CO2	Analyze ECG and EEG signal with characteristic feature points.	4	Analyzing
CO3	Model a biomedical system.	6	Creating

CO – PO Mapping :

PO	1	2	3	4	5	6
CO1			2			
CO2				2		
CO3						1
3-H, 2-M, 1-L						

Assessments :

Teacher Assessment:

Two components of In Semes Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) havin 0%, 30% and 50% weights respectively.

Assessment	Marks
ISE 1	10
MSE	30
ISE 2	10
ESE	50

ISE 1 and ISE 2 are based on assignment/declared test/quiz/seminar etc.
MSE: Assessment is based on 50% of course content (Normally first three modules)
ESE: Assessment is based on 100% course content with60-70% weightage for course content (normally last three modules) covered after MSE.

Course Contents:	
Module 1 : Introduction to Biomedical Signals	**Hrs.**
Introduction to Biomedical Signals, The nature of Biomedical Signals, Examples of Biomedical Signals, Objectives and difficulties in Biomedical analysis, Signal Conversion Systems, Conversion requirements for biomedical signals, Signal conversion circuits. Application areas of Bio -Signal analysis – EEG, ECG, Phonocardiogram, Spiro Gram, Evoked Signals.	**7**
Module 2 : Signal Averaging and Data Compression Techniques	**Hrs.**
Basics of signal averaging, signal averaging as a digital filter, a typical averager, software for signal averaging, limitations of signal averaging. Turning point algorithm, AZTEC algorithm, Fan algorithm, Huffman coding	**6**
Module 3 : Adaptive Noise Cancellation	**Hrs.**
Adaptive interference / Noise cancellation: Types of noise in biosignals; Digital filters - IIR and FIR - Notch filters - Optimal and adaptive filters. Weiner filters - steepest descent algorithm - LMS adaptive algorithm - Adaptive noise canceller - cancellation of 50 Hz signal in ECG - Cancellation of maternal ECG in foetal electrocardiography.	**6**
Module 4 : Cardiological signal processing	**Hrs.**
Basic Electrocardiography, ECG data acquisition, ECG lead system, ECG signal characteristics (parameters and their estimation), Analog filters, ECG amplifier, and QRS detector, Power spectrum of the ECG, Bandpass filtering techniques, Differentiation techniques, Template matching techniques, A QRS detection algorithm, Realtime ECG processing algorithm, ECG interpretation, ST segment analyzer, Portable arrhythmia monitor.	**7**
Module 5 : Neurological signal processing	**Hrs.**
Neurological signal processing: The brain and its potentials, The electrophysiological origin of brain waves, The EEG signal and its characteristics (EEG rhythms, waves, and transients), Correlation. Analysis of EEG channels: Detection of EEG rhythms, Template matching for EEG, spike and wave detection	**6**
Module 6 : Modeling of Biomedical Systems	**Hrs.**
Motor unit firing pattern, Cardiac rhythm, Formants and pitch of speech, Point process, Parametric system modeling, Autoregressive model, Autocorrelation method, Application to random signals, Computation of model parameters, Levinson-Durbin algorithm, Computation of gain factor,	**8**

Covariance method, Spectral matching and parameterization, Model order selection, Relation between AR and Cepstral coefficients.	

Modulewise Measurable Students Learning Outcomes :
After completion of respective modules, Students will be able to -
Module 1: gain insight into different biomedical signals
Module 2 & 3: get introduced to signal processing techniques to improve biomedical signals
Module 4 & 5 : understand applications of signal processing in Cardiology and Neurology
Module 6: design algorithm for modeling of biomedical systems.

Title of the Course and Course Code: **Professional Elective 2:Embedded Linux Programming 4EN516**	**L**	**T**	**P**	**Cr**
	3	0	0	3

Pre-Requisite Courses: Nil

Textbooks:

1. Christopher Hallinan, *"Embedded Linux Primer: A Practical Real-World Approach",* Prentice Hall; 1st edition (September 28, 2006), ISBN 978-0137017836
2. Richard Stones, Neil Matthew, *"Beginning Linux Programming"*, Wiley; Fourth edition (2008)
3. Felix Alvaro, "LINUX: Easy Linux For Beginners", Amazon.com
4. Karim Yaghmour, Jon Masters, Gilad Ben-Yossef, Philippe Gerum, *"Building Embedded Linux Systems",* O'Reilly Media; Second Edition (August 22, 2008) ISBN: 978-0596529680

References:

1. P. Raghavan, Amol Lad, Sriram Neelakandan, *"Embedded Linux System Design and Development",* Auerbach Publications; 1 edition (December 21, 2005), ISBN: 978-0849340581
2. http://crashcourse.ca/introduction-Linux-kernel-programming-2nd-edition
3. Anand Iyer, Director, Calypto Design Systems, NPTEL Course: "*Linux Programming & Scripting*", by Online Course on YouTube and Also on http://nptel.ac.in, L1-4, L7 and L43

Course Objectives :

1. To make students familiar with installation and use of the embedded Linux operating system
2. To facilitate the students to learn the fundamentals of Linux as applied to embedded hardware
3. To give exposure to system design using embedded Linux as per the industry trends.

CO-PO Mapping : Use H: High **M:** Moderate **L:**Low **for mapping;**

PO	**1**	**2**	**3**	**4**	**5**	**6**
CO1			2			
CO2				2		
CO3						1
3-H, 2-M, 1-L						

Assessments

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weights respectively.

ISE 1: 10 Marks to be submitted before MSE marks. It is open to students.

ISE 2: 10 Marks to be submitted before ESE. It is hidden component for students.

MSE: 30 Marks to be submitted within 10 days after MSE examination is over
(Generally on module 1-3)

ESE: 50 Marks to be submitted within 10 days after ESE examination
(60-70% weight for module 4-6 and 30-40% on module 1-3)

Course Contents:

Module 1: Introduction	**Hrs.**
Introduction to Linux, Linux Distributions, Open source Software, GPL, Facilities in Embedded Linux Boards used in Industry/Market, Important Accessories of Linux boards available/used in industry, Care to take in handling the Linux boards, Development Setup for EL, OS installation, init process, initrd, boot loaders, lilo and GRUB boot loaders, Case studies of Embedded Linux Based Systems	**5**
Module 2: Linux file system and commands	
Linux File System, Permissions, CLI and Linux Shells, Linux Commands, Linux concepts, Shell Script, Basic Linux system administration tasks on the RPi. Linux commands for file and process management. Linux Programming, Multi-file C programming Using make utility, Makefile, GNU debugger. Transferring Files Between Systems**,** Kernel, building kernel image.	**6**
Module 3: Multithreading and Hardware Access:	
Threads and processes, Multithreaded C programming. EL hardware design issues, Logic-level translation circuitry. Case studies of hardware of frequently used interfaces, Communication with EL board through network, EL GPIO control using sysfs, wiringPi and python. Python libraries	**7**
Module 4: Hardware Interfacing and Programming-I	
Using onboard I2C, SPI, and UART capabilities. Circuits to the RPi that interface to its I2C bus, Linux I2C-tools. Communicate between UART devices using both Linux tools and custom C or Python code. Interface to a low-cost GPS sensor using a UART connection. Extend the input/output capability using external serial ADCs, DACs, Increase the number of available GPIOs on the RPi using both I2C and SPI GPIO expanders.	**7**
Module 5: Hardware Interfacing and Programming-II	
Using Interrupt functionality on devices. Increasing the number of available serial UART devices on the RPi using low-cost USB-to-TTL devices. USB Bluetooth adapter for the RPi and connect to it from a mobile device for the purpose of building a basic remote-control application. Using Wi-Fi and Xigbee along with EL board. Hardware design for given system specifications.	**7**
Module 6: Basic Image Processing on Embedded Linux:	
Camera interfacing to EL board, Capture image and video. Stream video data to the Internet using Linux applications and UDP, multicast, and RTP streams. Using OpenCV to perform basic image processing on the RPi. Use OpenCV to perform a computer vision face-detection task. Play audio data on the using HDMI audio and USB audio adapters.	**7**

Module wise Measurable Students Learning Outcomes:

At the end of each module the students will be able to,

Module 1: Apply the basic concepts of Linux for various case studies.

Module 2: Apply the basic and frequently required Linux commands and shell scripting for basic administration

Module 3: Write, compile multi-file, multi-threaded programs using make and debug using gdb.

Module 4: Write programs to access and control the on board as well as outside hardware such as such as I2C/SPI/ GPIO/ Keyboard/LCD/Serial port etc. Design external hardware for EL board.

Module 5: Write programs for extending EL hardware and modules such as Wi-Fi module.

Module 6: Write OpenCV program for basic image processing using Linux.

Title of the Course and Course Code: Electronics Lab 2 4EN552	L	T	P	Cr
	0	0	4	2

Pre-Requisite Courses: Digital VLSI Design Lab

Reference Books:

1. Cadence manual
2. Microwind manual
3. Lab General manual

Course Objectives:

1. Demonstrate the flow of following EDA tools for designing digital circuits
   a. Microwind for designing digital circuits at physical level
   b. Cadence flow (Schematic entry to simulation) for implementing CMOS digital circuits
2. Prepare the students for executing an individual or group problem of medium complexity.

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive	
		Level	Descriptor
CO1	**Design** and **Simulate schematics** of CMOS circuits using Cadence tools and 90 nm technology	6^{th} (Creating)	Design and Simulate PO3
CO2	Design and simulate physical layouts with optimum area for gates, pass-T, TX gates etc using microwind tools	6^{th} (Creating)	
CO3	**Formulate** a research a problem, design, build and simulate either a researched problem or assigned by the supervisor in Digital VLSI Design area independently, submit a written report in standard format and demonstrate the simulation results with justification.	6^{th} (Creating) Skills viz. Research Life long learning & communication skills and ethics	

CO-PO Mapping :

PO	1	2	3	4	5	6
CO1			3			
CO2				3		
CO3	**2**					
3-H, 2-M, 1-L						

Lab Assessment:

There are four components of lab assessment, LA1, LA2, LA3 and Lab ESE.
IMP: Lab ESE is a separate head of passing.

Assessment	Based on	Conducted by	Conduction and Marks Submission	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 4 Submission at the end of Week 5	25
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 5 to Week 8 Submission at the end of Week 9	25
LA3	Lab activities, attendance, journal	Lab Course Faculty	During Week 10 to Week 14 Submission at the end of Week 14	25
Lab ESE	Lab Performance and related documentation	Lab Course faculty	During Week 15 to Week 18 Submission at the end of Week 18	25

Week 1 indicates starting week of Semester.
Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments.

Proposed List of experiments:

A: Using cadence Design Tools:

1. NMOS and PMOS characterization
2. Implementation of CMOS inverter and its characterization for VTC and power
    a. Equal area approach
    b. Equal delay approach
3. Implementation of 2-inpout NAND and NOR
    a. Finding out rise time, fall time of the output and propagation delay (50% input to
    b. 50% output) High-to-Low and Low-to-High
    c. Comparison of both for delay and power
4. Implementation of 1-bit full adder using carry-out of the stage to drive the sum output (28 transistor implementation)
5. Implementation of 2-input NAND and NOR gates using different logic styles and compare the performance parameters with complementary CMOS logic style
    a. Pseudo logic style
    b. Pass Transistor logic style
    c. Transmission gate logic style
    d. Differential cascade voltage switch logic
    e. Dynamic (pre-charge and evaluate) logic style
6. Implementation of transmission gate based full adder circuit
7. Implementation of four bit Manchester carry chain
8. Implementation of 4-bit barrel shifter using pass transistors

B. Demonstration of Microwind tool for layout by explaining DRC and simulation,

9. Implementation of inverter, 2 input NAND gate and any other circuit for practice

C. Task/miniproject/research problem:

For the last lab session which students will have to carry out a task for a period of at least six weeks it is recommended that:

1. Student can search or teacher can assign a course related medium complexity task to a group of student not exceeding two by defining the problem statement suitably.
2. Student has to submit a report/Journal consisting of appropriate documents – Abstract, Certificate of Completion by the supervisor, Table of Contents, Abbreviations, and other sections/chapters viz. Introduction, Motivation, Objectives, Outcomes, Brief theoretical Background, Problem Analysis, Design Aspects, Algorithms, Mathematical Model, Test Strategy, Results, Result Analysis and Conclusions and Future Scope) in the institute level standard format.
3. Cadence tools or other similar EDA tools are to be used for designing and implementing the designs and the report is to be written in standard IEEE format preferably using Latex.