Walchand College of Engineering, Sangli

(Government Aided Autonomous Institute)

Course Contents (Syllabus) for

Final Year B. Tech.
(Electronics Engineering)
Sem – VII to VIII

AY 2020-21

Title of the Course: Real Time Operating System 3EN401	**L-** 3	**T-** 0	**P-**0	**Cr-** 3

Pre-Requisite Courses:

Courses with C programming, Microcontroller, Peripherals and Interfacing, Embedded System Design

Textbooks:

1. *"MicroC OS II: The Real Time Kernel"* Jean J. Labrosse, CMP books ISBN: 978-1578201037

2. *"Real-Time Concepts for Embedded Systems"*, Qing Li, CarolineYao Elsevier
   ISBN: 978-1578201242

3. *"Simple Real-time Operating System: A Kernel",* Chowdary Venkateswara Amazon,
   ISBN: 978-1425117825

References:

1. www.micrium.com for uCOS-II related documents, tutorials, downloads.
2. www.nxp.com for processor specific documents.
3. www.wikipedia.org for general OS related basic literature.
4. www.NPTEL.org for OS and RTOS related video courses.

Course Objectives :

1. To explain/illustrate/demonstrate need of RTOS and services provided by it.

2. To explain/illustrate/demonstrate services provided by RTOS and their implementation

3. To explain/illustrate/demonstrate how to design of applications using RTOS.

(The RTOS used is uCOS-II as a case study).

Course Learning Outcomes:

CO	**After the completion of the course the student should be able to**	Bloom's Cognitive	
		level	Descriptor
CO1	**Apply** the knowledge of RTOS to decide whether a given system is suitable for RTOS based implementation.	2	Apply
CO2	**Apply** the theory and implementation of task, time and event management, inter-task communication and memory management.	2	Apply
CO3	**Analyze** the given program/problem or **solve** given RTOS based problem by **Applying** the theoretical knowledge acquired.	4	Analyze
CO4	**Design** the tasks and their interactions by using appropriate uCOS-II services for writing application programs for a given multitasking based (RTOS based) embedded system.	6	Create

CO-PO Mapping : Use H: High **M:** Moderate **L:**Low **for mapping;**

	1	2	3	4	5	6	7	8	9	10	11	12	PSO1	PSO2
CO1	H												M	
CO2	M												M	
CO3		H											H	
CO4			H											H

Assessments

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weights respectively.

ISE 1: 10 Marks to be submitted before MSE marks.

ISE 2: 10 Marks to be submitted before ESE.

MSE: 30 Marks to be submitted within 10 days after MSE examination is over (Generally on module 1-3)

ESE: 50 Marks to be submitted within 10 days after ESE examination (60-70% weight for module 4-6 and 30-40% on module 1-3)

Course Contents:

Module 1: Real-time Systems Concepts (6)

Foreground/Background Systems, Multitasking, Kernels, Priority inversion, Synchronization, Intertask communication, Advantages and disadvantages of real time kernel.

Module 2: Task management in uCOS-II (5)

uCOSII initialization, creating and deleting a task, changing task priority, suspending and resuming a task.

Module 3: Time and Event management in uCOS-II (8)

Clock tick, delaying a task, resuming the delayed task, getting system time, case study of application based on time management, initializing an ECB, making a task wait for an event, making a task ready on occurrence of event and timeout.

Module 4: Semaphore and Mutex in uCOS-II (7)

Creating and deleting a semaphore, waiting and signaling semaphore, creating and deleting mutex, waiting and signaling mutex, case study of application based on semaphore and mutex.

Module 5: Mail box and Message queue in uCOS-II (7)

Creating and deleting a mailbox, sending and receiving a message using mail box, using mailbox as binary semaphore, creating and deleting message queue, sending and receiving a message using message queue, case study of application based on mailbox and message queue.

Module 6: Event flag and Memory management in uCOS-II (6)

Creating and deleting event flag group, waiting and signaling an event flag, memory control block, creating a partition, obtaining and returning memory block, case study of application based on event flag and memory.

Module wise Measurable Students Learning Outcomes

Module 1: Classify RTOS and explain services provided by RTOS

Module 2: Explain implementation details of task and task management in uCOS-II

Module 3: Illustrate how time and events are handled by uCOS-II

Module 4: Explain and use semaphore and mutex, Solve problems using semaphores

Module 5: Explain and use mail box and message queue, Solve problems using mailbox and queue

Module 6: Explain the basics of event flag and memory management.

Title of the Course: 3EN402 **Computer Network and Protocols**	**L- 3**	**T- 1**	**P-**	**Cr- 4**

Pre-Requisite Courses: Digital Communication

Textbook:

1. "Data Communication and Networking" ,TMH, B. Forouzan
2. "TCP/IP Protocol Suite", TMH, B. Forouzan

References:

1. "Internetworking with TCP/IP", Pearson, Douglas Comer

Course Objectives :

1. To explain concept of Data Communication
2. To provide function of different layers
3. To demonstrate and analysis of TCP/IP protocol suite and networking

Course Learning Outcomes:

CO	**After the completion of the course the student should be able to**	Bloom's Cognitive	
		level	Descriptor
CO1	**Illustrate** data communication and networking concepts	2	Understanding
CO2	**Explain** detail protocol functionality and working	2	Understanding
CO3	**Analyze** higher layer protocols and design security for specific applications	4	Analyzing
CO4	**Analyze** application layer protocols and perimeter security	4	Analyzing

CO PO Mapping

	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
CO1	M											
CO2			M									
CO3		H										

CO4	M											

Assessments

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weights respectively.

ISE 1: 10 Marks to be submitted before MSE marks. It is open to students.

ISE 2: 10 Marks to be submitted before ESE. It is hidden component for students.

MSE: 30 Marks to be submitted within 10 days after MSE examination is over (Generally on module 1-3)

ESE: 50 Marks to be submitted within 10 days after ESE examination (60-70% weight for module 4-6 and 30-40% on module 1-3)

Course Contents:	
Module 1:Introduction Introduction to Network, Communication tasks, Transmission media, Topology, Switching. Circuit switching, message switching, packet switching, TDM, FDM, OSI Model, TCP/IP Model Comparison, Networking components.	6
Module 2: Data Link Layer Data Link layer design issues, Logical Link Control, Medium Access Control, Elementary Data link layer protocols, Sliding window protocol , Medium access sub layer- Multiple access protocols.	7
Module 3:Network Layer (IP) Logical Addressing, IPV4, Address space, Class-full Classless addressing, Network Address Translation (NAT), Internet protocol, fragmentation, Address Mapping (ARP, RARP), ICMP-Types of messages ,Message formats, Error Reporting, Query Routing, introduction to IPV6	7
Module 4: Transport Layer (TCP/ UDP) Duties of Transport layer, Process to Process delivery, User Datagram Protocol, Transmission Control Protocol TCP, Flow Control, Error Control, Congestion control in TCP, TCP Timers	6
Module 5: Application Layer Domain Name System (DNS) - Name space, Distribution of Name space Resolution, Remote Login-TELNET, concept of Network Virtual Terminal (NVT), File Transfer Protocol (FTP), SNMP, Email SMTP, POP, IMAP, Introduction to Multimedia RTP, RTCP.	7
Module 6: Security(Firewall, Firewall types configurations, IPSec, VPN), Bluetooth, BLE, CAN, ZigBee, MODBUS like industrial protocols.	6

Module wise Measurable Students Learning Outcomes Module 1 Describe fundamentals of data communication and networking Module 2 Explain Data link layer in detail Module 3Explain addressing and routing in networking. Module 4 Explain TCP and UDP Module 5Analyse Application layer Protocol Module 6 Analysis of security and other industrial Protocol	

Professional Core (Lab)

Title of the Course: 3EN451 Real Time Operating System Lab	**L-** 0	**T-** 0	**P-**2	**Cr-** 1

Pre-Requisite Courses:

Theory/Lab Courses with C programming, Microcontroller Peripherals and Interfacing, Embedded System Design

Textbooks:

1. *"MicroC OS II: The Real Time Kernel"* Jean J. Labrosse, CMP books publication ISBN: 978-1578201037
2. *Lab Manual*

References:

5. www.micrium.com for uCOS-II related documents, tutorials, downloads.
6. www.nxp.com for processor specific documents

Course Objectives :

1. To give the students practical experience of RTOS and services provided by it.

2. To expose the students to RTOS implementation and internal operation of RTOS.

3. Give exposure to and facilitate the students for write applications using RTOS.

(The RTOS used is uCOS-II as a case study).

Course Learning Outcomes:

CO	**After the completion of the course the student should be able to**	Bloom's Cognitive	
		level	Descriptor
CO1	**Apply** the theoretical knowledge and demonstrate the basics of RTOS and the acquired skills of managing uCOS-II based project. (Practical Experience, Modern Tools)	2	Apply
CO2	**Write** programs to prove/verify the theory and demonstrate usage of task, time and event management, Intertask communication.(Programming skill, Modern Tools)	6	Create
CO3	**Analyze** given RTOS based problem by applying the theoretical knowledge acquired.(Problem Solving, Modern Tools)	4	Analyze
CO4	**Implement** a given logic as an RTOS based application. Create document of the same and demonstrate using simulation tools. (Programming skill, Independent and team work, Modern Tools)	6	Create

CO-PO Mapping : Use H: High **M:** Moderate **L:**Low **for mapping;**

	1	2	3	4	5	6	7	8	9	10	11	12	PSO1	PSO2
CO1	**H**				H								**M**	
CO2		**H**			H									**H**
CO3		**H**			H								**H**	
CO4			H		H									**H**

Lab Assessment:

There are four components of lab assessment, LA1, LA2, LA3 and Lab ESE.

IMP: Lab ESE is a separate head of passing.

Assessment	Based on	Conducted by	Conduction and Marks Submission	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 4 Submission at the end of Week 5	25
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 5 to Week 8 Submission at the end of Week 9	25
LA3	Lab activities, attendance, journal	Lab Course Faculty	During Week 10 to Week 14 Submission at the end of Week 14	25
Lab ESE	Lab Performance and related documentation	Lab Course faculty	During Week 15 to Week 18 Submission at the end of Week 18	25

Week 1 indicates starting week of Semester.
Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course.

The experimental lab shall have typically 8-10 experiments.

List of Experiments:

1. Study of an RTOS based application
2. Proving that uCOS-II is a preemptive RTOS
3. Semaphore for managing shared resource and task synchronization
4. Clock tick and its accuracy in RTOS
5. Semaphore for event synchronization
6. Using mail box facility in RTOS
7. Use of queue facility in RTOS (Self-study)
8. Use of dead-lock in RTOS
9. Verifying priority inversion in RTOS (Self-study)
10. Mini-Project (Solving given problem by writing relevant program, Simulation, documentation, Demonstration)

The mini-project should be based on some product requirement that involves need of virtual parallelism, scalability, shared resource, inter-task communication etc. The project should use maximum facilities in the RTOS such as semaphore, mailbox, queues etc. The mini-project is to be completed using uVision4 (demo) for developing the code and Proteus simulator for hardware simulation.

Title of the Course: **3EN491 Project I**	L	T	P	Cr
	0	0	8	4

Pre-Requisite Courses:

Textbooks:

1. Electronics Projects For Dummies, by by Earl Boysen and Nancy Muir, Published by Wiley Publishing, Inc., 2006
2. Make: Electronics, by Charles Platt, Published by Maker Media, 2015

References:

1. A. E. Ward, J.A.S. Angus, "Electronic Product Design", Stanley Thrones (Publishers) Limited, 1996.
2. Paul Horowitz, Winfield Hill, "The Art of Electronics", Cambridge University Press, 1989

Course Objectives :

1. To provide students hands on experience on, troubleshooting, maintenance, fabrication, innovation, record keeping, documentation etc thereby enhancing the skill and competency part of technical education
2. To create an Industrial environment and culture within the institution.
3. To inculcate innovative thinking and thereby preparing students for main project.
4. To set up self-maintenance cell within departments to ensure optimal usage of infrastructure facilities.

Course Learning Outcomes:

CO	**After the completion of the course the student should be able to**	Bloom's Cognitive level	Descriptor
CO1	Choose, Initiate and manage a minor project.	I	Remembering
CO2	Propose research problem and present them in a clear and distinct manner through different oral, written and design techniques.	VI	Creating
CO3	Construct, Comment and Evaluate Mini Projects' undertaken/ implemented by other students.x	VI	Creating

CO-PO Mapping :

PO	1	2	3	4	5	6	7	8	9	10	11	12	PSO1	PSO2
CO1		**3**											**2**	**2**
CO2			3											**2**
CO3			3											**2**

1- Low , 2 – Medium, 3 – High

Assessments :

Lab Assessment:

There are four components of lab assessment, LA1, LA2, LA3 and Lab ESE.

IMP: Lab ESE is a separate head of passing.

Assessment	Based on	Conducted by	Conduction and Marks Submission	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 4 Submission at the end of Week 5	25
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 5 to Week 8 Submission at the end of Week 9	25
LA3	Lab activities, attendance, journal	Lab Course Faculty	During Week 10 to Week 14 Submission at the end of Week 14	25
Lab ESE	Lab Performance and related documentation	Lab Course faculty	During Week 15 to Week 18 Submission at the end of Week 18	25

Project Description

A project group shall consist of *not more than 3 students* per group. The mini project will involve the design, construction, and debugging of an electronic system approved by the department. Each student should conceive, design develop and realize an electronic product. The electronic part of the product should be an application of the analog & digital systems covered up to the 7^{th} semester. The schematic and PCB design should be done using any of the standard schematic capture & PCB design software. . The realization of the product should include design and fabrication of PCB.

Each student must keep a project notebook/logbook. The project notebooks will be checked periodically throughout the semester, as part of in-semester-evaluation. The student should submit a soft bound report at the end of the semester. The final product as a result of project should be demonstrated at the time of examination.

Broad Areas of Project

The Projects may be from the following areas/domains, but not limited to:

- Embedded Systems
- Electronic Control Systems
- Electronic Communication Systems
- Biomedical Electronics
- Power Electronics
- Robotics and Mechatronic Systems
- Electric Vehicles
- Artificial Intelligence and Machine Learning
- Applications of Electronics to Agriculture

ASSESSMENT

A demonstration and oral examination on the mini project **shall be conducted at the** end of the semester. The examination will consist of demonstration and viva voce on the project.

Professional Elective (Theory)

Professional Elective IV

Title of the Course: 3EN411 Analog VLSI Design	**L-** 3	**T-** 0	**P-**0	**Cr-** 3
Pre-Requisite Courses: CMOS VLSI Design				
Textbooks: 1. " Behzard Razavi, *Design of Analog CMOS Integrated Circuits*, , TATA McGraw-Hill Publication, Eight Edition onwards (2005)				

References:

1. R. Jacob Baker, *CMOS, Circuit Design, Layout and Simulation*, Wiley-Inter- science, (2008)
2. Allen, P.E. and Holberg, D.R., *CMOS Analog Circuit Design*, Oxford University Press (2002)
3. Web-sites: vlsi.expert.com, testbench.in, asic-world.com

Course Objectives :

1. To explain the analog circuit concepts based on MOS devices in such a way to develop in students the insight and intuition towards MOS circuits
2. To organize guest lectures and practical sessions with the help of industry persons.
3. To deliver the tips (or thumb rules) related with design of analog circuits throughout the course
4. To motivate the students to develop lifelong/self learning attitude.

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive level	Descriptor
CO1	**Analyze** MOS device circuits to derive the dependence of various electrical parameters analytically and graphically. (M1)	4th (Analyzing)	Analyze
CO2	**Develop** large signal and small signal models for single stage amplifiers and differential amplifiers using MOS transistors and derive the gain relationships (M2. M3)	3rd (Applying)	Develop
CO3	**Design** common source, common gate, common drain amplifier for given specifications. Further recognize their application under various typical situations. (M2, M3)	3rd (Applying)	Design
CO4	**Analyze** large signal and small signal behavior of differential amplifiers and compute the differential gain, common mode gain and CMRR. (M3)	4th (Analyzing)	Analyze
CO5	**Analyze** active current mirrors and explain the properties of differential pairs using such circuits as loads. (M4)	4th (Analyzing)	Analyze
CO6	**Compute** the poles and zeros in the frequency response of the single stage amplifiers using time-constant method (M5)	3rd (Applying)	Compute
CO7	**Design** 2-stage Op-Amp for given specifications..(M6)	3rd (Applying))	Design

CO-PO Mapping : Use H: High **M:** Moderate **L:**Low **for mapping;**

	1	2	3	4	5	6	7	8	9	10	11	12
CO1												
CO2												
CO3												
CO4												
CO5												
CO6												
CO7												

Assessments

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ISE 1: 10 Marks to be submitted before MSE marks. It is open to students.

ISE 2: 10 Marks to be submitted before ESE. It is hidden component for students.

MSE: 30 Marks to be submitted within 10 days after MSE examination is over (Generally on module 1-3)

ESE: 50 Marks to be submitted within 10 days after ESE examination (60-70% weight for module 4-6 and 30-40% on module 1-3)

Course contents:

Module 1:

MOS Device Physics:

MOS IV Characteristics, Second Order Effects, MOS device models (MOS device capacitance, MOS small signal model) MOS model parameters

Module 2:

Single Stage Amplifier: Part I

CS stage with resistance load, diode connected load, current source load, , CS stage with source

degeneration,	
Module 3: Single Stage Amplifier: Part II source follower, common-gate stage, cascode stage, folded cascade, choice of device models.	
Module 4: Differential Amplifiers: Basic difference pair, differential mode response, common mode response, Differential pair with MOS loads	
Module 5: Passive and Active Current mirrors: Basic current mirrors, Cascode mirrors, active current mirrors.	
Module 6: Frequency Response:: CS stage, Source follower, Common gate stage, Cascode stage and Difference pair.	
Operational Amplifiers: Design of 2-stage operational amplifier	

Title of the Course: 3EN412 **System on Chip**	**L- 3**	**T-0**	**P- 0**	**Cr-3**

Pre-Requisite Courses:

Textbook:

1. FPGA based system design by Wyne wolf – published by prentice hall.
2. Readings in hardware/software co-design Giovanni De Micheli,Rolf Ernst, and Wayne Wolf – published by Morgan Kaufman.
3. Computers as components: Principles of embedded computing system design published by Morgan Kaufman publishers

References:

1. Multiprocessors systems-on-chips by Ahmed jerrya wayne wolf,eds- Morgan Kaufman publishers
2. Core connect architecture at http://www.chips.IBM.com/products/coreconnect
3. EDK power PC tutorial at http://www.xilinx.com/EDK
4. Power PC info http://www.chips .IBM.com/products power PC/cores/405sde_pb.html.
5. Arm processor details at WWW.arm.com
6. AMBA bus architecture at http://www.arm.com/products/solutions/Ambahomepage.html http://www.princeton.edu/~wolf

Course Objectives :

1. To make students aware of the system on chip concepts and bus system
2. To make students learn the hardware-software co-design approach
3. To make student learn embedded soft processors
4. To make students learn Model-based system design with modern tools

Course Learning Outcomes:

CO	**After the completion of the course the student should be able to**	Bloom's Cognitive	
		level	Descriptor
CO1	understand concepts of SOC and SOC bus sub system	2	Explain, Demonstrate
CO2	apply knowledge of embedded soft processors while designing SOC	3	Develop, Build
CO3	analyze and design SOC by high end software tools	4	Examine , Discover
CO4	Design SOC based system using different programming languages	5	Create, Design, Develop

CO PO Mapping

	a	**b**	**c**	**d**	**e**	**f**	**g**	**h**	**i**	**j**	**k**
CO1	**x**										
CO2											

CO3											
CO4											

Assessments

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ESE: 50 Marks to be submitted within 10 days after ESE examination (60-70% weight for module 4-6 and 30-40% on module 1-3)

Course Contents:

Module 1:
Concept of system, importance of system architectures, introduction to SIMD, SSID, MIMD and MISD architectures, concept of pipelining and parallelism. Designing microprocessor /Microcontroller based system and embedded system..

Module 2:
Introduction to SOC, Differences between Embedded systems and SOCs. Introduction to busses used in SOCs, Introduction to AMBA bus, IBM's core connect bus, concept of PLB-processor local bus and OPB-on chip peripheral bus, System design issues in SOCs.

Module 3:
Concept of Soft embedded processors. Study of Microblaze RISC processor. Study of IBM's power PC

Module 4:
Programmable logic and FPGA Architecture. Study of Latest FPGA Architecture. Study of features like embedded Block RAMs, multipliers, Digital clock management, CPU cores etc. Introduction to tools used for SOC design, Xilinx/ Altera embedded development kit

Module 5:
Design Flow for SOC design. Using existing IP Blocks in SOC design, Designing new peripheral IP with AXI bus, Embedded programming with SOC.

Module 6:
SOC system design example with Peripherals like USB, UART, Ethernet Etc. using latest FPGA. (Xilinx/ Altera tools) Eclipse IDE development tool for a full SOC system design with embedded C/C++ applications (Xilinx/ Altera tools)

Module wise Measurable Students Learning Outcomes

Module 1, 2:

Module 3 :

Module 4 :

Module 5, 6:

Title of the Course:	L	T	P	Cr
Elective : **3EN413Microwave Communication**	3		0	3

Pre-Requisite Courses:

Textbooks:

1. *"Microwave Devices and Circuits", Samuel* Y. Liao, PHI.

2. *"Microwave Engineering", 3rd Edition,* Manojit Mitra, Dhanpat Rai & Co.

References:

1. *"Microwave Engineering",* D. M. Pozar, John Wiley.

2. *"Electronics Communication Systems",* George Kennedy, Tata McGraw Hill.

Course Objectives :

1. To understand the theoretical principles underlying microwave devices and networks
2. To introduce the various types of transmission lines and to discuss the losses associated
3. To instill knowledge on the properties of various microwave components
4. To deal with the microwave generation and microwave measurement techniques

Course Learning Outcomes:

CO	**After the completion of the course the student should be able to**	Bloom's Cognitive level	Descriptor
CO1	Classify the microwave frequencies and the waveguides that are used application	2	Classify
CO2	Categories the propagation of signals through antenna	4	Categories
CO3	Examine the active & passive microwave devices & components used in Microwave communication systems	4	Examine
CO4	Analyze the operation and working of the various tubes or sources for the transmission of the microwave frequencies	4	Analyze

CO-PO Mapping : Use H: High **I:** Intermediate/Moderate **B:** Basic/Low **for mapping;**

Please do not tick

	a	**b**	**c**	**d**	**e**	**f**	**g**	**h**	**i**	**j**	**k**	**PSPO**
CO1	**I**											
CO2		**H**										
CO3			H									
CO4							H					

Assessments: Teacher Assessment:

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weights respectively.

Assessment	Marks
ISE 1	10
MSE	30
ISE 2	10
ESE	50

ISE 1 and ISE 2 are based on assignment/declared test/quiz/seminar etc.
MSE: Assessment is based on 50% of course content (Normally first three modules)
ESE: Assessment is based on 100% course content with 60-70% weightage for course content (normally last three modules) covered after MSE.

Course Contents:

Module 1	**6Hrs.**
Module 1: Microwave Fundamentals and Electromagnetic field Theory Microwave regions and band designations, microwave devices, applications of microwaves, Interaction between electrons and fields, electron motion in electric, magnetic and electromagnetic field, electromagnetic plane waves	
Module 2	**6Hrs.**
Module 2: Microwave Waveguide and Components Rectangular and circular waveguide, TE and TM modes, power transmission and power losses in waveguide, excitation modes in waveguide, microwave cavities, Microwave passive components—Tee junctions, magic tee, couplers, circulators, attenuators, phase shifters, bends, twists, corners, irises, windows. Scattering Matrix Parameters of microwave networks, S-matrix for E-plane Tee junction, S-matrix for H-plane Tee junctions, S-matrix for directional coupler.	
Module 3	**8Hrs.**
Module 3: Microwave Tubes Limitations of conventional tubes, O and M type classification of microwave tubes, reentrant cavity, velocity modulation. **O type tubes**	

Two cavity Klystron: Construction and principle of operation, velocity modulation and bunching process Applegate diagram. **Reflex Klystron**: Construction and principle of operation, velocity modulation and bunching process, Applegate diagram, Oscillating modes, o/p characteristics, efficiency, electronic & mechanical tuning. **M-type tubes** **Magnetron**: Construction and Principle of operation of 8 cavity cylindrical travelling wave magnetron, hull cutoff condition, modes of resonance, PI mode operation, o/p characteristics, Applications. **Slow wave devices** Advantages of slow wave devices, **Helix TWT**: Construction and principle of operation, Applications.	
Module 4	**8Hrs.**
Module 4: Microwave Solid State Devices Tunnel diode, PIN diode, Gunn diode, LSA diode, Read diode, IMPATT diode, TRAPATT diode, BARITT DIODE, Varactor Diode, solid state ruby laser, semiconductor laser.	
Module 5	**6Hrs.**
Module 5: Microwave Measurements Measurement devices: Slotted line, Tunable detector, VSWR meter, Power Meter, S-parameter measurement, frequency measurements, Power measurement, Attenuation measurement, Phase shift measurement, VSWR measurement, Impedance measurement, Q of cavity resonator measurement	
Module 6	**6Hrs.**
Module 6: Microwave Strip Lines and Antenna Micro-strip line, Slot line, Parallel strip line, advantages, Horn antenna, Dish Antenna, Micro-strip antenna	

Professional Elective V

Title of the Course: 3EN414 **Digital System Engineering**	**L-** 3	**T- 1**	**P-**0	**Cr-4**

Pre-Requisite Courses:

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Textbooks:

1. 1. *Digital System Engineering",* William Dally and John Poulton, Cambridge University Press, Reprint 2007

References:

1. *"High Speed Digital Design"*- A Handbook of Black Magic, Howard W. Johnson, Martin Graham, Prentice Hall PTR, Englewood Cliffs, NJ 0763
2. *"High Speed Digital System Design*: Interconnect Theory and Design Practices" Stephen H. Hall, Garrett W. Hall, James A. McCall, Wiley-IEEE Press (ISBN: 978-0-471-36090-2
3. Net material on Clock distribution and power distribution

Course Objectives :

1. To explain the effect of parasitic of wires/interconnects in restricting the high speed performance of digital circuits and design the approaches to tackle this problem by using their engineering models.
2. To discuss and explain the different sources of interference (noise) in digital systems and apply engineering/statistical models of these to compute and compare bit error rates.
3. To illustrate the significance of signaling & timing issues in high speed digital design and select a proper one for error-free transfer of information (bits) from one location to another.
4. To compare Meso-chronous, Plesio-chronous and fully synchronous systems and to design synchronizers to avoid Meta-stability problems of fully synchronous systems. To explain further self timed circuits as a good alternative to synchronous circuits.

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive level	Descriptor
CO1	**Analyze** the effect of parasitic of wires/interconnects in restricting the high speed performance of digital circuits and **design** the approaches to tackle this problem by using their engineering models. (M1)	IV Analyzing	Analyze
CO2	**Explain** different sources of interference (noise) in digital systems and **apply** engineering/statistical models of these to compute and compareBER(M2)	III Applying	Explain
CO3	**Compare and contrast** different signaling & timing approaches and choose the one for **designing** error-free transfer of information (bits) from one location to another. (M3, M4, M5)	IV, V Analyzing and Evaluating	Compare and Design
CO4	**Explain** various types of digital systems and **design** synchronizers to avoid meta stability problems of fully synchronous systems. (M6)	III Applying	Design

CO-PO Mapping : Use H: High **M:** Moderate **L:**Low **for mapping;**

	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
CO1												
CO2												
CO3												
CO4												

Assessments

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weights respectively.

ISE 1: 10 Marks to be submitted before MSE marks. It is open to students.

ISE 2: 10 Marks to be submitted before ESE. It is hidden component for students.

MSE: 30 Marks to be submitted within 10 days after MSE examination is over (Generally on module 1-3)

ESE: 50 Marks to be submitted within 10 days after ESE examination (60-70% weight for module 4-6 and 30-40% on module 1-3)

Course contents:

Module1: 6

Wires: Geometrical and Electrical properties, Electrical models of wires (Ideal wire, Transmission

line), Simple transmission lines (RC, lossless LC, lossy LRC transmission lines, Dielectric absorption),	
Module 2: **Noise in Digital Systems**: Noise sources in a digital system, Power Supply Noise, Cross-talk, Inter-symbol Interference, Managing noise.	7
Module 3: **Signaling Conventions Part I**: CMOS and Low swing current mode signaling system, Considerations in transmission system design, Signaling modes for transmission lines, Transmitter signaling methods,	6
Module 4: **Signaling Conventions part II** :, Receiver signal detection, Source termination, Under-terminated Drivers, Differential Signaling, Signaling over capacitive transmission medium, Signal encoding	4
Module 5: **Timing Conventions**: Conventional Synchronous system and closed loop pipelined system, Considerations in timing design, Timing fundamentals, Timing properties of combinational logic and clock storage elements, Eye diagram, Encoding Timing (Signals and Events), Open loop synchronous timing, Closed loop timing,	8
Module 6: **Synchronization**: Synchronization Fundamentals, Applications of synchronization (Arbitration of asynchronous signals, Sampling asynchronous signals, Crossing clock domains), Synchronization failure and meta-stability, Synchronizer Design	8

Title of the Course: 3EN415 Mobile Communication Engineering	L	T	P	Cr
	3	1	0	4

Pre-Requisite Courses: Probability Theory and statistics, Digital Communication Engineering

Textbooks:

1. *"Wireless Communications Principles and Practice"*, II Ed. PHI ,T.S.Rappaport
2. "*Principle and Application of GSM*", V.K.Garg, J.E.Wilkes, Pearson Education

References:

1. *"Mobile Cellular Telecommunications Systems*", WCY Lee McGraw Hill Publication.
2. "*A GSM system Engineering*", Asha Mrhrotra, Artech House Publishers Bosten, London.

Course Objectives :

1. To describe mobile cellular communication systems over mobile radio environment
2. To illustrate evolution of different generations of mobile networks.
3. To explain different multiple access technologies.

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive	
		Level	Descriptor
CO1	Apply concepts in mobile communications to analyze its effects on interference, system capacity, handoff techniques	3	Applying
CO2	Distinguish various multiple-access techniques for mobile communications	4	Analyzing
CO3	Analyze and design GSM system knowing system architecture, mapping of functional layers, different Call flows.	4	Analyzing
CO4	Use advanced principles and technique to design appropriate mobile communication systems.	3	Applying

Assessments :

Teacher Assessment:

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weights respectively.

Assessment	Marks
ISE 1	10
MSE	30
ISE 2	10
ESE	50

ISE 1 and ISE 2 are based on assignment/declared test/quiz/seminar etc.

MSE: Assessment is based on 50% of course content (Normally first three modules)

ESE: Assessment is based on 100% course content with60-70% weightage for course content (normally last three modules) covered after MSE.

Course Contents:

Module 1 : Cellular Communication Fundamentals	**Hrs.**
Introduction of Cells, Channel Reuse, SIR Calculations, Traffic Handling Capacity: Erlang Performance, Cellular system design, Co channel interference ratio, Co channel interference reduction techniques and methods to improve cell coverage, Frequency management and channel assignment, concepts of cell splitting, handover in cellular system.	**7**
Module 2 : Multiple access technologies	**Hrs.**
Frequency Division Multiple access (FDMA), Time Division Multiple access (TDMA), Code Division Multiple access (CDMA), spectral efficiency calculations, comparison of T/F/CDMA technologies based on their signal separation techniques, advantages, disadvantages and application areas.	**6**
Module 3 : GSM Architecture and Interfaces	**Hrs.**
Introduction to GSM subsystems, GSM Interfaces, GSM architecture, details of following blocks in GSM (Mobile station, Base station systems, Switching subsystems, Home location registers, Visiting location registers, Equipment identity register, Echo canceller), Mapping of GSM layers onto OSI layers, GSM Logical Channels, Data Encryption in GSM, Mobility Management, Call Flows in GSM. Mobile Management: Handoff, Location and Paging	**8**
Module 4 : Mobile Radio Propagation	**Hrs.**
Large Scale Path Loss, Free Space Propagation Model, Reflection, Ground Reflection (Two-Ray) Model, Diffraction, Scattering, Signal Penetration into Buildings. Small Scale Fading and Multipath Propagation, Impulse Response Model,Types of Small Scale Fading: Time Delay Spread, Doppler Spread.	**6**

Module 5 : Higher Generation Cellular Standards	**Hrs.**
2.5 G Standards: High speed Circuit Switched Data (HSCSD), General Packet Radio Service (GPRS), 2.75 G Standards: EDGE.	**7**
Module 6 : 3G and 4G Wireless Standards	**Hrs.**
Evolution of IS 95 (cdmaOne)to cdma 2000, WCDMA, LTE, WiMAX	**6**

Module wise Measurable Students Learning Outcomes :

Module 1: Student will gain insight into the theoretical framework and the core concepts of the wireless mobile networks

Module 2: Student will get introduced to multiple access technologies for wireless network

Module 3: Student will equip with understanding of the various concepts various concepts of GSM

Module 4: Students will get knowledge characteristics of the mobile radio environmental propagation phenomena.

Module 5: Students will get understanding of evolution of mobile networks.

Module 6: Students will get introduced to different 3G and 4G wireless standards.

Title of the Course and Course Code: 2EN 417 Wireless Sensor Network (Professional Elective V)	L	T	P	Cr
	3	1	-	4

Pre-Requisite Courses: Fundamentals of networking.

Textbooks:

1. Kazem Sohraby, Daniel Minoli, Taieb Znati, "Wireless Sensor Networks Technology Protocols and Applications", John Wiley & Sons Inc. Publication ,2007

References:

1.Edgar H. Callaway, Jr. and Edgar H. Callaway, "Wireless Sensor Networks: Architectures and Protocols" ,CRC Press, August 2003
2. Ian F. Akyildiz, Mehmet Can Vuran,"Wireless Sensor Networks" ,John Wiley & Sons Ltd. 2010

Course Objectives :

1.To explain the Wireless Sensor Network and its applications
2.To distinguish working principles of various WSN protocols
3.To discuss security issues of WSN and its performance

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive	
		Level	Descriptor
CO1	Analyse Prototypes for Wireless Sensor Network	Analyzing	Distinguish
CO2	Calculate performance issues in Wireless Sensor Network	Evaluating	Justify
CO3	Analyse different layer protocols and security issues of Wireless Sensor Network	Analyzing	Identify

Assessment:

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weightage respectively.

Assessment	Marks
ISE 1	10
MSE	30
ISE 2	10
ESE	50

ISE 1 and ISE 2 are based on assignment, oral, seminar, test (surprise/declared/quiz), and group discussion.[One assessment tool per ISE. The assessment tool used for ISE 1 shall not be used for ISE 2]
MSE: Assessment is based on 50% of course content (Normally first three modules)
ESE: Assessment is based on 100% course content with70-80% weightage for course content (normally last three modules) covered after MSE.

Course Contents:

Module 1 :Introduction and Overview of Wireless Sensor Networks	Hrs.
Introduction to wireless Ad-hoc network , Mobile Ad-hoc Network and Overview of Wireless Sensor Networks, Applications of Wireless Sensor Networks	5
Module 2:Wireless Transmission Technology and Medium Access Control Protocols	Hrs.
Basic Wireless Sensor Technology, Sensor Node Technology, Hardware and Software, Sensor Taxonomy, Wireless Transmission Technology and Systems, Medium Access Control Protocols for Wireless Sensor Networks, Fundamentals of MAC Protocols, MAC Protocols for WSNs.	7
Module 3: Routing Protocols and Transport Control Protocols for Wireless Sensor Networks	Hrs.
Routing Challenges and Design Issues in Wireless Sensor Networks, Routing Protocols for Wireless Sensor Networks, -Data Dissemination and Gathering, , Routing Strategies in Wireless Sensor Networks, Transport Control Protocols for Wireless Sensor Networks, Traditional Transport Control Protocols, Transport Protocol Design Issues, Examples Transport Control Protocols	9
Module 4: Middleware and Network Management for WSN	Hrs.
WSN Middleware Principles- Middleware Architecture, Existing Middleware, Network Management for Wireless Sensor Networks Operating Systems for Wireless Sensor Networks- Operating System Design Issues and Examples	7
Module 5: Security Issues	Hrs.
WSN security issues, Possible attacks on WSN, worm hole, black hole , sync attack and effect on performance, mitigation techniques	6
Module 6: Performance and Traffic Management	Hrs.
Performance and Traffic Management- Introduction, Background, WSN Design Issues, Performance Modelling of WSNs, Performance Metrics, Basic Models, Network Models	5

Module wise Measurable Students Learning Outcomes :

Module 1: Distinguish different types of ad hoc networks and its applications

Module 2: i)Analyze wireless sensor node components , transmission impairments and performance issues
ii)Analysis of MAC protocols

Module 3: i)Distinguish Routing protocols and Transport control protocol for WSN

Module 4: i)Describe of middleware and network management protocols
ii)Design issues of OS for WSN

Module 5: Identify different security issues of WSN

Module 6: Analyse Different models of WSN and its performance analysis.

Professional Elective (Lab)

<table>
<tr><td colspan="3">Title of the Course: 2EN452 Analog VLSI Design Lab</td><td>L-0</td><td>T-0</td><td>P-2</td><td>Cr-1</td></tr>
<tr><td>References:</td><td colspan="6">Text Books:

1. Behzard Razavi, Design of Analog CMOS Integrated Circuits, , TATA McGraw-Hill Publication.
2. Cadence Lab Manual: White papers from Cadence
3. WCE Laboratory Manual : (in-house prepared)
Reference Books:

2. R. Jacob Baker, CMOS, Circuit Design, Layout and Simulation, Wiley-Inter- science, (2008)
3. Allen, P.E. and Holberg, D.R., CMOS Analog Circuit Design, Oxford University Press (2002)
4. Web-sites: vlsi.expert.com, testbench.in, asic-world.com</td></tr>
<tr><td>Course Objectives :</td><td colspan="6">1. Demonstrate the flow of Cadence EDA tools for designing and simulating analog CMOS circuits.
2. Develop an insight into CMOS analog circuits and design single stage CS, CG, CD, differential amplifiers and 2-stsge Operational amplifier for given specifications.
3. Explain how to characterize the transistors for the voltage conditions seen by the circuit with goal of optimizing dimensions for given ID or trans-conductance.
4. Prepare the students for good documentation discipline.</td></tr>
<tr><td rowspan="6">Course Learning Outcomes</td><td>CO</td><td colspan="2">At the end of the course, student will be able to</td><td colspan="2">Bloom’s Cognitive</td></tr>
<tr><td></td><td colspan="2"></td><td>Level</td><td>Descriptor</td></tr>
<tr><td>CO1</td><td colspan="2">Characterize MOS transistors for targeted value of gm or drain current for designing the physical dimensions and the required gate bias using Cadence EDA tools.</td><td>III Applying</td><td>Characterize</td></tr>
<tr><td>CO2</td><td colspan="2">Demonstrate the complete flow of Cadence tools from schematic to symbol generation to simulation for CS, CG, CD and differential amplifiers</td><td>Skills

Use of Modern Tools</td><td>Demonstrate</td></tr>
<tr><td>CO3</td><td colspan="2">Build and simulate the single stage amplifier circuits (CS, Source Follower, Cascode stage, differential pair etc.) using MOSFETs schematic design entry for various loads and relate the gain values with theoretical expressions.</td><td>IV, V

Analyzing and Evaluating</td><td>Build and Simulate</td></tr>
<tr><td>CO4</td><td colspan="2">Design differential pair circuits with active current mirror load for given gain and UGB.</td><td>III Applying</td><td>Design</td></tr>
<tr><td>CO5</td><td colspan="2">Design, build and simulate 2-stage operational amplifier for given pole frequencies and UGB with and without pole splitting and pole-zero compensation.</td><td>III , V Applying,</td><td>Design, Build,</td></tr>
</table>

			Evaluating	Simulate
	CO6	Exhibit following technical and professional skills. Hands on skills of using modern EDA tools, Communication Skills, Collaborative work spirit Research Skills, Lifelong learning attitude Ethical behavior	VI Related with psychomotor and affective domain and assessed thr' rubric on a scale of 1 to 5	
		Laboratory Outcomes	Maps to CO	Maps to PO
Specific laboratory outcomes	LO1	Design and Simulate schematics of CMOS circuits using Cadence tools and 180 nm technology (CO1)	CO1	PO1 (3)
	LO2	Implement the Cadence flow from schematic entry to simulation for single stage amplifiers of various topologies, differential amplifier and 2-stage op-amp. (CO2 to CO5)	CO2 to CO5	PO1(3)
	LO3	Exhibit following skills (CO6)	CO6	Psychomotor and affective domain as above
		A) Hands on skills on EDA tools		
		B) Written communication skills		
		C) Oral Communication skills		
		D) Group/team (collaborative) work spirit		
		E) Research Skills		
		F) Life long Learning Attitude		
		G) Ethical Behaviour		

Lab Assessment:

There are four components of lab assessment, LA1, LA2, LA3 and Lab ESE.

IMP: Lab ESE is a separate head of passing.

Assessment	Based on	Conducted by	Conduction and Marks Submission	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 4 Submission at the end of Week 5	25
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 5 to Week 8 Submission at the end of Week 9	25

LA3	Lab activities, attendance, journal	Lab Course Faculty	During Week 10 to Week 14 Submission at the end of Week 14	25
Lab ESE	Lab Performance and related documentation	Lab Course faculty	During Week 15 to Week 18 Submission at the end of Week 18	25

List of Experiments:

Lab No	Details	Skill Developed
1	Characterize nMOS transistors from schematic using Cadence tools	Use of Modern Tools
2, 3	Design, build and simulate Single stage amplifier Common source amplifier using resistive load and nMOS diode connected load. (Gain and Frequency response) Compare the performance with pMOS diode connected load	Application of knowledge to design and evaluate (Third Bloom's level)
4	Design, build and simulate Common Source amplifiers with current source load Compare the performance with already studied loads .	
5	Design, build and simulate Common source stage with source degeneration. (gain and frequency response) Compare the performance with and without source degeneration	Application of knowledge to design and evaluate (Third Bloom's level)
6	Design, build and simulate Source follower / Common Gate stage Crosscheck the results of output impedance, gain, power dissipation against theoretical expectations	
7	Design, build and simulate cascode stage with different loads for specified voltage gain and maximum power dissipation.	Application of knowledge to design and evaluate (Sixth Bloom's level)
8,9	Design, build and simulate differential pair with specified tail current source and maximum full swing differential gain using a)resistive load and b) pMOS current source load and compare the gain values. Cross-confirm the results against theoretical expectations.	Application (3^{rd}) Evaluation (6^{th})
	Demonstrate design of differential pair with active tail current source (replace the tail current source in Expt. 8 by a nMOS current source biased in saturation. Simulate for evaluating differential gain , common mode gain and CMRR.	Use of Modern tools Evaluation (6^{th})
10	Design, build and simulate differential amplifier (single ended output) with active current mirror load for the given specifications. Evaluate for CMRR, DC gain etc.	Application Evaluation
	Demonstrate design of 2-stage operational amplifier for given UGB	

Title of the Course: 2EN454 Microwave Communication Lab	**L-** 0	**T-** 0	**P-**2	**Cr-** 1

Pre-Requisite Courses:

Textbooks:

1. *"Microwave Devices and Circuits", Samuel* Y. Liao, PHI.

2. *"Microwave Engineering", 3rd Edition,* Manojit Mitra, Dhanpat Rai & Co.

References:

1. *"Microwave Engineering",* D. M. Pozar, John Wiley.

2. *"Electronics Communication Systems",* George Kennedy, Tata McGraw Hill.

Course Objectives :

1. To understand the theoretical principles underlying microwave devices and networks
2. To introduce the various types of transmission lines and to discuss the losses associated
3. To instill knowledge on the properties of various microwave components

To deal with the microwave generation and microwave measurement techniques

Course Learning Outcomes:

CO	**After the completion of the course the student should be able to**	Bloom's Cognitive	
		level	Descriptor
CO1	Classify the microwave frequencies and the waveguides that are used application	2	Classify
CO2	Categories the propagation of signals through antenna	4	Categories
CO3	Examine the active & passive microwave devices & components used in Microwave communication systems	4	Examine
CO4	Analyze the operation and working of the various tubes or sources for the transmission of the microwave frequencies	4	Analyze

CO-PO Mapping : Use H: High **M:** Moderate **L:**Low **for mapping;**

	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
CO1				H								

CO2				**H**								
CO3				H								
CO4				H								

Assessments

Lab Assessment:

There are four components of lab assessment, LA1, LA2, LA3 and Lab ESE.

IMP: Lab ESE is a separate head of passing.

Assessment	Based on	Conducted by	Conduction and Marks Submission	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 4 Submission at the end of Week 5	25
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 5 to Week 8 Submission at the end of Week 9	25
LA3	Lab activities, attendance, journal	Lab Course Faculty	During Week 10 to Week 14 Submission at the end of Week 14	25
Lab ESE	Lab Performance and related documentation	Lab Course faculty	During Week 15 to Week 18 Submission at the end of Week 18	25

List of Experiments:

Microwave Engineering Lab

List of Experiments:

1. Study of Microwave components and equipment

2. Study of V-I Characteristics of Gunn Diode

3. Reflex Klystron as source and plot its various modes

4. Verification of port characteristics of E-plane tee, H-plane tee & Magictree

5. Verification of port characteristics of Microwave Circulator and isolator, calculation of insertion loss and isolation loss

6. Verification of port characteristics of Directional coupler, calculation of coupling factor, insertion loss and directivity.

7. Power pattern of Horn Antenna

8. Power Patterns of different Antenna like Dipole, Yagi etc.

9. Study of slotted section with probe carriage. Measure the VSWR for various values of terminating impedances (open/short/matched termination).

10. To test and verify Microwave Integrated Circuits using Microstrip trainer kit and finds parameters, and plot the frequency response.

Title of the Course and Course Code: 2EN453 System On Chip Lab	L	T	P	Cr
	0	0	2	1

Pre-Requisite Courses: Microprocessor / Microcontrollers

Textbooks:1. Michael J Flynn and Wayne Luk, —Computer system Design: System-on-Chip , Wiley-India, 2012.

2. Sudeep Pasricha and Niki Dutt, —On Chip Communication Architectures: System on Chip Interconnect , Morghan Kaufmann Publishers, 2008.

3.Lin, Y-L S (ed.), —Essential Issues in SOC Design: Designing Complex Systems-on-chip. Springer, 2006.

References: 1. Wolf W H, —Computers as Components: Principles of Embedded Computing System Design , Elsevier, 2008.

2. Patrick Schaumont —A Practical Introduction to Hardware/Software Co-design , Patrick Schaumont, Springer, 2012.

3. Lin, Y-L S (ed.), —Essential Issues in SOC Design: Designing Complex Systems-on-chip. Springer, 2006. 6. Wayne Wolf, —Modern VLSI Design: IP Based Design , Prentice-Hall India, 2009.

4. Amba bus architecture at http://www.arm.com/products/solutions/Ambahomepage.html

Course Objectives :

1. To make students aware of the system on chip concepts

2. To make students learn the Bus interconnect hardware Design approach

3. To make students learn the IP design

4. To make students learn Model-based system design

5. To make students learn hardware software co-design approach

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive	
		Level	Descriptor
CO1	Design using interconnect bus like AMBA for SoC technology	Creating	Design
CO2	Design IPs using EDA Tools	Creating	Design
CO3	Design SoC for given specifications and implement using EDA Tools.	Creating	Design
CO4	Discuss the test strategy, write the test benches and test the designed SoC for functionality and performance using EDA Tools	Creating	Discuss, Test

CO-PO Mapping :

	1	2	3	4	5	6	7	8	9	10	11	12	PSO1	PSO2
CO1	3													
CO2		3												
CO3				2										
CO4														**2**

Assessment:

Lab Assessment:

There are four components of lab assessment, LA1, LA2, LA3 and Lab ESE.

IMP: Lab ESE is a separate head of passing.

Assessment	Based on	Conducted by	Conduction and Marks Submission	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 4 Submission at the end of Week 5	25
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 5 to Week 8 Submission at the end of Week 9	25
LA3	Lab activities, attendance, journal	Lab Course Faculty	During Week 10 to Week 14 Submission at the end of Week 14	25
Lab ESE	Lab Performance and	Lab Course faculty	During Week 15 to Week 18	25

	related documentation		Submission at the end of Week 18	

Week 1 indicates starting week of Semester.
Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course.

The experimental lab shall have typically 8-10 experiments.

Course Contents:

1. Demonstrate AMBA Bus
2. Design and execute GPIO IP program with 8 bit port
3. Design and execute PWM IP program with 4 channels
4. Design and execute UART IP program
5. Design and execute SPI bus IP
6. Design and execute SOC with various IP
7. Design and execute SOC for DSP applications
8. Design and execute SOC for Image processing applications

Experiment wise Measurable Students Learning Outcomes : students will

Experiment 1: Demonstrate the SOC hardware Design approach

Experiment 2: Design GPIO IP using EDA tool

Experiment 3: Design PWM IP using EDA tool

Experiment 4: Design UART IP using EDA tool

Experiment 5: Design SPI bus IP using EDA tool

Experiment 6: Design SOC using EDA tool

Experiment 7: Design SOC for DSP using EDA tool

Experiment 8: Design SOC for Image processing using EDA tool

Open Elective III

Title of the Course: 4OE 457 **Cyber Physical System**	L	T	P	Cr
	3	0	0	3

Pre-Requisite Courses: Signals and Systems

Textbooks: (NOT MORE THAN 3)

1. Introduction to Cyber physical systems
2. The Internet of Things key applications and protocols, Olivier Hersent, David B. Omer Elloumi, Wiley publications

References: (NOT MORE THAN 3)

1. http://www.cyphylab.ee.ucla.edu
2. Smart Grid Applications, Communications, and security edited by Lars T Berger K Iniewski, Wieley Publications

Course Objectives :

1. To illustrate the fundamental concepts of Cyber Physical Systems

2. To explain design of Cyber Physical Systems.

3. To enable the students for the design and development of CPS

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive	
		level	Descriptor
CO1	Explain fundamentals and components of CPS	II	Understanding
CO2	Analyze the components of CPS	IV	Analyzing
CO3	Design the CPS Systems for given Applications	VI	Creating
CO4			

CO-PO Mapping :

	a	**b**	**c**	**d**	**e**	**f**	**g**	**h**	**i**	**j**	**k**	**l**
CO1	M											
CO2		H										
CO3				M								
CO4												

Assessments :

Teacher Assessment:

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weights respectively.

Assessment	Marks
ISE 1	10
MSE	30
ISE 2	10
ESE	50

ISE 1 and ISE 2 are based on assignment/declared test/quiz/seminar etc.

MSE: Assessment is based on 50% of course content (Normally first three modules)

ESE: Assessment is based on 100% course content with60-70% weightage for course content (normally last three modules) covered after MSE.

Course Contents:

Module 1 : Introduction	**Hrs.**
Introduction of Cyber Physical Systems, various components of CPS, Applications of Cyber Physical System, Design aspects of Cyber Physical system, Introduction to Real Time System	4 Hrs
Module 2 : **Sensing**	
Types of sensors, Classifications of sensors, Different selection criteria of sensors, Sensor Instrumentation, Concept of Smart sensors, Wireless sensors	6 Hrs
Module 3 : **Sensor Network and Protocols**	
Sensor Network, Wireless Sensor Network, working of WSN, routing in wireless sensor network, Gateway functions, Data Aggregations, design issues of WSN Short distance protocols : Bluetooth, BLE (Bluetooth Smart), Zigbee, and Industrial protocol Modbus, Mbus, 6LoWPAN, IEC68XX	9 Hrs
Module 4: Embedded system computing	
Introduction to Embedded system, Architecture, Programming aspects, peripherals and system design,	6Hrs
Module 5: CPS Security	
CPS security, Holistic Approach to Security, Overview of Security Technologies Principal security requirements, Security Issues, Types of attacks to CPS.	6 Hrs
Module 6: CASE Study	
Industry Automation, Smart Grid, SCADA, general case study of any CPS.	9 Hrs

Module wise Measurable Students Learning Outcomes :

Module 1: Students will become familiar with components of Cyber Physical System

Module 2: Students will get introduced to basic structures for sensing system

Module 3: Students will be able to understand WSN and protocols

Module 4: Students will be able to understand embedded system concepts.

Module 5: Students will understand security issues and mitigation system of CPS

Module 6: Students will analyze detail CPS structure.

Final Year Electronics SEM VIII

Engineering Management, and Ethics

Professional Elective VI

Title of the Course: 3EN431 VLSI in Digital Signal Processing	L	T	P	Cr
	3	0	0	3

Pre-Requisite Courses:

Textbooks:

1. *"VLSI Digital Signal Processing- Design and Implementation" ,* Keshav K. Parhi, Wiely (India) 2007

References:

1. *"VLSI Synthesis of DSP kernels- Algorithms and Architectural Transformations",* Mahesh Mehendale, Sunil Sherlekar, Kluwer Publications, 2002

Course Objectives :

1. Understand the basic parameters like critical period, loop bound, iteration bound etc. from architecture point of view to design high speed digital systems for DSP applications. (L2)
2. Understand various approaches like pipelining, parallel processing, retiming, unfolding, folding etc to optimize above performance parameters for high speed digital systems without ignoring area and power minimization objective. (L2, L3)
3. To apply and synthesize above algorithms for few cases and to compare and contrast the merits and demerits of each algorithm. (L3, L4, L5)
4. To develop and enrich the computer libraries with functions implementing above algorithms for future use in designing and developing high speed digital systems. (L4)
5. To design a digital system (as a mini-project) for any high frequency applications taking into consideration any of the above algorithms. (L6)
6. Nurture an attitude to work in teams and develop written as well as oral presentation skills.

Course Learning Outcomes:

CO	After the completion of the course the student should be able to	Bloom's Cognitive	
		Level	Descriptor
CO1	Define and describe critical period, loop bound, iteration bound etc.	II	Understand
CO2	Apply various approaches like pipelining, parallel processing, Retiming, Unfolding, Folding, Systolic Array etc. for designing high speed and high throughput, energy efficient digital systems	III	Apply
CO3	Implement above algorithms for few cases and compare merits and demerits of each algorithm	III	Apply
CO4	Work in Team for solving and writing assignments	III	Apply

CO-PO Mapping :

	1	2	3	4	5	6	7	8	9	10	11	12
CO1	L											
CO2	M		H									
CO3	L	M	H									
CO4						M		M				

Assessments : Teacher Assessment:

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weights respectively.

Assessment	Marks
ISE 1	10
MSE	30
ISE 2	10
ESE	50

ISE 1 and ISE 2 are based on assignment/declared test/quiz/seminar etc.

MSE: Assessment is based on 50% of course content (Normally first three modules)

ESE: Assessment is based on 100% course content with60-70% weightage for course content (normally last three modules) covered after MSE.

Course Contents:

Module 1 DFG Representation and Iteration Bound	**Hrs.**
Representations of DSP algorithms Critical Period, Loop bound, Iteration bound, LPM and MCM algorithms	**7**
Module 2 Pipelining and Parallel Processing	**Hrs.**
Pipelining approach to reduce critical path Parallel Processing to handle higher sample rates , Power Reduction computations, Combined pipelining and Parallel processing	**7**
Module 3 Retiming	**Hrs.**
Introduction to Retiming (Definitions and properties), Solving system of inequalities, Cutset Retiming and Pipelining, Retiming for clock period minimization ,Retiming for register minimization	**7**

Module 4 Unfolding	**Hrs.**
Introduction to Unfolding ,Algorithm for unfolding, Properties of unfolding, Sample Period Reduction, Word level and bit-level parallel Processing	**7**
Module 5 Folding	**Hrs.**
Introduction to folding, Folding Transformation, Lifetime Analysis for Register minimization in folded architecture, Folding of multi-rate DSP systems	**7**
Module 6 Systolic Array Design	**Hrs.**
Methodologies, Family of systolic arrays (FIR filter) using linear mapping techniques, Matrix – Matrix Multiplication	**6**

Module wise Measurable Students Learning Outcomes : After the completion student should be able to

1. develop graphical models
2. understand basic performance parameters
3. develop logical skills & enable to understanding and knowledge, Compare and contrast skills
4. develop analytical and computational skills & enable to apply knowledge in practical
5. develop analytical and optimization skills
6. develop cognitive skills for design methodologies; enable to apply systolic array knowledge for general application

Title of the Course:	L	T	P	Cr
3EN432 : Satellite Communication	3	0	0	3

Pre-Requisite Courses:

Textbooks:

1. Satellite Communications Dennjs Roddy, 2nd Edition, 1996, McGraw Hill.
2. Satellite Communications —Timothy Pratt, Charles Bostian, Jeremy Allnutt, 2nd Edition, 2003, John Wiley & Sons.

References:

1. Satellite Communications: Design Principles — M. Richcharia, 2nd Ed., BSP, 2003.
2. Fundamentals of Satellite Communications — K. N. Raja Rao, PHI, 2004.Course Outcome

Course Objectives :

5. To prepare students to excel in basic knowledge of satellite communication principles
6. To provide students with solid foundation in orbital mechanics and launches for the satellite communication
7. To train the students with a basic knowledge of link design of satellite with a design examples.
8. To provide better understanding of multiple access systems and earth station technology
9. To prepare students with knowledge in satellite navigation and GPS & and satellite packet communications

Course Learning Outcomes:

CO	**After the completion of the course the student should be able to**	Bloom's Cognitive	
		level	Descriptor
CO1	Analyze satellite orbit	4	Analyze
CO2	Analyze the earth segment and space segment	4	Analyze
CO3	Design various satellite applications	4	Design

CO-PO Mapping : Use H: High **I:** Intermediate/Moderate **B:** Basic/Low **for mapping;**

Please do not tick

	a	**b**	**c**	**d**	**e**	**f**	**g**	**h**	**i**	**j**	**k**	**PSPO**
CO1	**H**			H								
CO2	**H**											
CO3			H									

Assessments: Teacher Assessment:

Two components of In Semester Evaluation (ISE), One Mid Semester Examination (MSE) and one End Semester Examination (ESE) having 20%, 30% and 50% weights respectively.

Assessment	Marks
ISE 1	10
MSE	30
ISE 2	10
ESE	50

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MSE: Assessment is based on 50% of course content (Normally first three modules)
ESE: Assessment is based on 100% course content with 60-70% weightage for course content (normally last three modules) covered after MSE.

Course Contents:

Module 1	**6Hrs.**
Module 1: Communication Satellite: Orbit and Description: A Brief history of satellite Communication, Satellite Frequency Bands, Satellite Systems, Applications, Orbital Period and Velocity, effects of Orbital Inclination, Azimuth and Elevation, Coverage angle and slant Range, Eclipse, Orbital Perturbations, Placement of a Satellite in a Geo-Stationary orbit.	
Module 2	**6Hrs.**
Module 2: Satellite Sub-Systems: Attitude and Orbit Control system, I I &C subsystem, Attitude Control subsystem, Power systems, Communication subsystems, Satellite Antenna Equipment. Satellite Link: Basic Transmission Theory, System Noise Temperature and G/T ratio, Basic Link Analysis, Interference Analysis, Design of satellite Links for a specified C/N, (With and without frequency Re-use), Link Budget.	
Module 3	**8Hrs.**
Module 3: Propagation effects: Introduction, Atmospheric Absorption, Cloud Attenuation, Tropospheric and lonospeheric Scintillation and Low angle fading, Rain induced attenuation, rain induced cross polarization interference.	
Module 4	**8Hrs.**
Module 4: Multiple Access: Frequency DivisIon Multiple Access (FDMA) – Intermodujation Calculation of C/N, Time Division Multiple Access (TDMA) – Frame Structure, Burst Structure, Satellite Switched TDMA, On-board Processing, Demand Assignment Multiple Access (DAMA) — Types of Demand Assignment, Characteristics, CDMA Spread Spectrum Transmission and Reception.	
Module 5	**6Hrs.**

Module 5: Earth Station Technology: Transmitters, Receivers, Antennas, Tracking Systems, Terrestrial Interface, Power Test Methods, Lower Orbit Considerations.		
Module 6	**6Hrs.**	
Module 6: Satellite Navigation and GPS Systems: Radio and Satellite Navigation, GPS Position Location Principles, GPS Receivers, GPS C/A Code Accuracy, Differential GPS.		