	Walchand College of Engineering, Sangli (Government Aided Autonomous Institute)									
			(0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	AY 2021-22						
			Cour	rse Information						
Progr	amme		M. Tech. (Electr	onics Engineering)						
Class,	Semes	ter	First Year M. Te	ech., Semester I						
Cours	e Code	2	5EN501	· · · · · · · · · · · · · · · · · · ·						
Cours	e Nam	e	FPGA based sys	tem design						
Desire	ed Reg	uisites:	Digital Electroni	ics, VLSI Design, N	ficrocontroller					
	-									
T	eachin	g Scheme		Examination	Scheme (Marks)					
Lectu	re	3 Hrs/week	T1	T2	ESE	Total				
Tutor	ial	-	20	20	60	100				
Practi	cal	-		<u> </u>	I					
Intera	ction	-		Cre	dits: 3					
			1							
			Cou	rse Objectives						
1	Unde	rstand Digital s	ystem design usin	g HDL.						
2	Knov	v FPGA archite	cture, interconnec	t and technologies.						
3	Knov	v different FPG	A's and implement	ntation methodologi	es.					
4	4 Configuring and implementing digital embedded system, microcontrollers, Microprocessors,									
	DSF		roa. se Outcomes (CC)) with Bloom's Ta	vonomy Level					
At the	end of	the course, the	students will be al	ble to,						
CO1	Com	pare various ty	pes of FPGA arch	itectures with justifi	cation	Understan d				
CO2	Deve	lop finite state	machines for vario	ous applications.		Apply				
CO3	Anal	yze the embedd	ed systems before	the actual product	is developed.	Analyze				
<u>CO4</u>	Desi	gn and develop	embedded system	using EDA tools.		Create				
Mada	1.		N. J			TT				
Modu		I CI Degign ou	MOG	iule Contents		Hours				
I	D an	igital system de	erview esign options and a, FPGA Architect	trade-offs, High Le ural options,	vel System Architecture	6				
II	H H n	ardware descri ardware descri achine design,	ription Languag ption languages, test benches	ge: Behavioural me combinational and	odelling and simulation, sequential design, state	6				
III	L F Ir	ogic block arcl PGA logic cell aput and Output	hitecture: s, timing models, cell characteristic	, power dissipation es, clock input, Timi	I/O block architecture: ng, Power dissipation	7				
IV	Simulation/implementation exercises: V Fast arithmetic logic blocks (Adders, Multipliers, ALUs), Data path controller 7 architecture. Scheduling and Allocation. Pipelining 7									
V	N F OI	lemory unit: ROM, SRAM, I rganization	DRAM, Virtual M	Iemory, Cache mer	nories, Paging, Memory	7				
VI	A E st	pplications: mbedded syster udies.	n design using FP	GAs, DSP using FP	GAs, application case	6				

	Text Books
1	FPGA Based Digital Design : Wayne Wolf, Pentice Hall, 2012
2	
	References
1	Digital System Design using VHDL, Charles H. Roth, PWS Publishing, a branch of
1	Thomson Learning
2	Clive Maxfield, "The Design Warriors's Guide to FPGAs", Elsevier, 2004.
2	Digital System Design using VHDL, Charles H. Roth, PWS Publishing, a branch of
5	Thomson Learning
4	FPGA product catalog from Xilinx and Altera
	Useful Links
1	https://nptel.ac.in/
2	https://www.coursera.org/
3	https://forums.xilinx.com/
4	

CO-PO Mapping															
		Programme Outcomes (PO) PSO													
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1			2												
CO2	2														
CO3				2											
CO4			2			2							1	1	
The strength of	f map	oping	is to	be wri	itten as	1,2,3;	Where	e, 1:Lo	w, 2:M	ledium	, 3:Hig	ŗh			

Each CO of the course must map to at least one PO.

Assessment Plan based on Bloom's Taxonomy Level								
Bloom's Taxonomy Level	T1	T2	ESE	Total				
Remember								
Understand	20		20	40				
Apply		10	20	30				
Analyze		10	20	30				
Evaluate								
Create								
Total	20	20	60	100				

	Walchand College of Engineering, Sangli (Government Aided Autonomous Institute)						
	AY 2021-22						
	Course Information						
Programme	M.Tech. (Electronics Engineering)						
Class, Semester	Class, Semester First Year M.Tech., Sem I						
Course Code	5EN502						

Course Name		Embedded System Design						
Desired Requ	isites:	Microprocessors / Microcontrollers						
Teaching S	cheme			Examinatio	n Scheme (Mar	·ks)		
Lecture	3 Hrs/we	ek	T1	T2	ESE	Tota	1	
Tutorial	-		20	20	60	100		
Practical	-				Nil			
Interaction	-				Credits: 3			
			Cou	irse Objectives				
1	Understa available	nd AR on va	RM processor of arious embedde	core architecture ed Cortex- M pr	e with several fe ocessors	atures of periph	erals	
2	Understa	nd inte	errupts and its	programming w	vith peripherals			
3	Develop application	small on soft	embedded sys tware for it	tem by using the	e ARM processo	or core based sy	stems and	
4	Use EDA	tools	to design emb	bedded system F	PCB.			
5	Interface	variou	us memories w	vith cortex M pr	ocessor			
	Co	ourse (Outcomes (CO	D) with Bloom'	s Taxonomy Lo	evel		
At the end of t	the course,	the stu	udents will be	able to,				
CO1	Illustrat	e Corte	ex M3 / M4 pr	ocessor archited	cture and its feat	tures	Underst and	
CO2	Apply pr interrupts	ogram S	nming skills to	develop algorit	hm for peripher	als and	Apply	
CO3	Develop	embec	dded system so	oftware.			Create	
CO4	Design a	nd dev	velop embedde	ed systems based	1 applications		Create	

Module	Module Contents	Hours
Ι	ARM Cortex –M Architecture and Programming ARM Cortex M3/M4 Architecture, Registers, CPU status, Clock generation, Memory organization, Instruction Set, Programming model – Registers, Operation Modes, Embedded C Programming	б
П	Cortex M CPU Interrupts Nested Vectored Interrupt Controller (NVIC), Vector table, Interrupt priorities, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency, Start-up files, initialization of peripherals interrupts, Interrupt routines programming	6

	ARM Peripherals and Programming	
	On chip peripherals, GPIO, RTC, Watchdog, UART, I2C, I2S, ADC and SPI	
III	interfacing and Programming, Repetitive interrupt timer, PWM Block	8
	programming, CAN BUS programming, LIN bus programming, DMA	
	programming, Writing LCD drives, Drivers for serial port communication	

IV	Peripheral Programming Design embedded system using Cortex-M3/M4 processors with SPI, UART, ADC, DAC, Memory, Timer, PWM peripherals.	8
V	Algorithm Designing and Debugging State Machine based Embedded Programming, Writing initialisation programs, Debugging techniques, Debugging with JTAG, Debugging with UART port, open source tools for software development	6
VI	Hardware design issues Selection of electronics components, Reading Schematic, Datasheets, footprints of various components, EDA tool for PCB design, Hierarchical design, Schematic and board layout design, board assembly process, board bring-up, cold and hot testing	6

The assessment is based on 2 in-semester examinations in the form of T1 (Test-1) and T2 (Test-2) of 20 marks each. Also there shall be 1 End-Sem examination (ESE) of 60 marks. T1 shall be typically on modules 1 and 2, T2 based typically on modules 3, 4 and ESE shall be on all modules with nearly 50% weightage on modules 1 to 4 and 50% weightage on modules 5, 6.

Text Books															
1	Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2nd Edition														
2	Frank Vahid and Tony Givargis, "Embedded System Design", Wiley														
							Ref	eren	ces						
1	Sloss	And	rew l	v, Sy	mes I	Domi	nic, V	Nrigh	nt Chi	ris, "A	ARM	Syste	em D)evel	oper's Guide:
1	Designing and Optimizing", Morgan Kaufman Publication														
2	Steve	e furb	er, "A	ARM	Syste	em-o	n-Chi	ip Ar	chited	cture'	', Pea	rson	Educ	atior	1
3	Frank	c Vah	id an	d To	ny Gi	varg	is, "E	mbec	lded S	Syste	m De	sign'	', Wi	ley	
4	Tech	nical	refer	ences	and	user	manu	als o	n ww	w.arr	n.cor	n, NX	KP Se	emico	onductor
	www	.nxp.	com	and T	Texas	Instr	umer	nts <u>w</u>	ww.ti	.com	, ST I	Micro	belec	tronic	cs <u>www.st.com</u>
	Useful Links														
1							1	VPTE	L Le	cture	5				
						С	O-PC) Ma	ppin	g					
				Prog	gram	me ()utco	mes	(PO)						PSO
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1			2												
CO2				2											
CO3	2			2											
CO4	2			2									1	1	
The	stren	gth o	f mar	ping	is to	be w	ritten	as 1,	,2,3; \	Wher	e, 1:I	Low,	2:Me	dium	n, 3:High
			Eac	h CC	of th	ne co	urse r	nust	map t	to at l	east o	one P	0.		

Assessment Plan based on Bloom's Taxonomy Level

Bloom's Taxonomy Level	T1	T2	ESE	Total
Remember	10			
Understand	10		20	
Apply		10	20	
Analyze		10	20	
Evaluate				
Create				
Total	20	20	60	100

[
Walchand College of Engineering, Sangli (Government Aided Autonomous Institute)								
			(Governing	AV 2021	-2.2.			
				Course Info	- 			
Prog	ramme	•	M Tech (F	lectronics Eng	vincering)			
Class	Semest	ér	First Year M	A Tech Sem]				
Cour	se Code		5EN560	1. reen., Benri				
Cour	se Nom	e	Research M	ethodology				
Dogirod	Doquisi	tos:	Nono	ethodology				
Desireu	Kequisi	1105.	None					
Teachi	ng Scha	mo			Examination Schom	o (Morks)		
Lootumo	ing Sche		Ι.Α.1	L A 2		Total		
Tutorial		-	20	LA2 20	40	100		
		-	30	30	40	100		
Practical		-			Nil			
Interaction	n	2 Hrs/week			Credits: 2			
				~				
				Course Obj	ectives			
1	To dev method	elop a researcl	n orientation a	among the stud	lents and to acquaint the	em with fundamentals of re	search	
2	To dev	elop understar	ding of the ba	asic framewor	k of research process an	d techniques		
3	To ide	ntify various so	ources of info	rmation for lit	erature review and data	collection.		
4 To develop an understanding of the ethical dimensions of conducting applied research.								
5	To dev	elop understar	ding about pa	atent process.				
		Cou	rse Outcome	es (CO) with I	Bloom's Taxonomy Le	vel		
At the end of the o	course, t	he students wi	ll be able to,					
CO1	Classi	fy various met	nods to solve	research probl	em.		Apply	
CO2	Const	ruct a research	problem in re	espective engi	neering domain.		Apply	
CO3	Invest	igate various d	ata analysis t	echniques for	a research problem.		Analyze	
CO4	Identi	fy various Intel	llectual Prope	rty Rights pro	cedures		Apply	
							11	
Module				Modu	ale Contents		Hours	
I		Research Fund What is resear Formulation o	damentals ch, types of r f a research p	esearch, the pr	rocess of research, Liter	ature survey and review,	4	
II		Research Met Research desig scaling technic	hods gn- Meaning, ques, Data Co	Need and Typellection – con	bes, Research Design P cept, types and methods	rocess, Measurement and s, Processing and analysis	5	
		of data, Design Analysis Tech Ouantitative T	n of Experime niques bechniques, Sa	ent ampling funda	mentals, Testing of hypo	othesis using various tests		
III III III IIII IIII IIIIIIIIIIIIIIII						5		
IV		Research Com Writing a con Presentation te of journal/con	munication ference paper, Journal Paper, Technical report, dissertation/thesis writing. echniques, software used for report writing such as WORD, Latex etc. Types ference papers					

V	Intellectual Property Rights Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development.	5			
	International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.	5			
VI	Patents and Patenting Procedures Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs				
	Text Books				
1	C. R. Kothari, Research Methodology, New Age international				
2	Deepak Chopra and Neena Sondhi, Research Methodology : Concepts and cases, Vikas Pu House, New Delhi	blishing			
	References				
1	E. Philip and Derek Pugh, How to get a Ph. D. – a handbook for students and their supervise university press	ors, open			
2 Stuart Melville and Wayne Goddard, Research Methodology: An Introduction for Science & F Students					
	Useful Links				
NDTEL Lectures					

CO-PO Mapping															
	Programme Outcomes (PO)											PSO			
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	2		1												
CO2					2	2									
CO3				2											
CO4						2									

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High Each CO of the course must map to at least one PO.

Assessment									
There are three components of lab assessment, LA1, LA2 and Lab ESE.									
IMP: Lab ESE is a separate head of passing. LA1, LA2 together is treated as In-Semester									
Evaluation.									
Assessme	Based on	Conducted Typical Schedule (for 26-week							
nt		by	Sem)	ks					
	Lab activities,	Lab Course	During Week 1 to Week 6						
LA1	attendance,	Lab Course	Marks Submission at the end of	30					
	journal	гасину	Week 6						

LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 7 to Week 12 Marks Submission at the end of Week 12	30
Lab ESE	Lab activities, attendance, journal	Lab Course Faculty	During Week 15 to Week 18 Marks Submission at the end of Week 18	40

Week 1 indicates starting week of a semester. The typical schedule of lab assessments is shown, considering a 26-week semester. The actual schedule shall be as per academic calendar. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments.

Assessment Plan based on Bloom's Taxonomy Level (Marks) (For lab Courses)										
Bloom's Taxonomy Level	LA1	LA2	Lab ESE	Total						
Remember										
Understand										
Apply	15			15						
Analyze	15	10		25						
Evaluate		10	20	30						
Create		10	20	30						
Total Marks	30	30	40	100						

Walchand College of Engineering, Sangli (Government Aided Autonomous Institute)									
AY 2021-22									
Course Information									
Programme	Programme M Tech (Electronics Engineering)								
Class. Semes	ster	First Year M 7	Tech Sem I	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,					
Course Code	ρ	5FN551							
Course Nam		Activity based	lah FPGA hase	d system design					
Desired Reg	Course maine Activity based fab 11 GA based system design Desired Dequisites: Image: Course of the system design								
Teachi	ing Scheme]	Examination Sc	heme (Marks)				
Lecture	-	LA1	LA2	ESE		Total			
Tutorial	-	30	30	40		100			
Practical				Ni	1				
2 H	Irs/week								
Interaction	-			Credi	ts: 1				
				•					
	m 1 . 1.1	D 1 (D 1	Course Of	ojectives	•				
	To understand the	e Product Devel	opment Process	through Mini Pr	oject.				
	To understand bu	dgeting through	Mini project	41					
3	To use different f	PGA's and imp	iementation me	thodologies.		Missona DCD			
4	To learn Configuring and implementing digital embedded system, microcontrollers, Microprocessors, DSP								
5	To understand the	e importance of	document desig	n by compiling '	Fechnical Report	t on the Mini Project work			
_	carried out.			,					
		Course Outee	mas (CO) with	Ploom's Taxon	omy Loval				
At the end of	the course the stu	dents will be abl	e to						
	Identify the rea	uirements for t	he real world i	problems		Analyze			
	Understand and	plan mini projec	t based on FPG	A based system	2	Apply			
<u> </u>	Design and build	the project su	ccessfully	in oused system	,	Design			
	Deliver technic:	al seminar hase	ed on the Mini	Project work c	arried out	Create			
CO4	Denver teenines	ai seinnai base		i loject work c		ciette			
			Guidelines for	Mini Proiect					
				•J•••					
1. The	students must under	rstand following	aspects while r	olanning Mini Pr	oject				
a. Co	oncept of FPGA's a	and implementat	tion methodolog	gies	5				
b. Im	portance								
c. Int	erdisciplinary								
d. Ch	nallenges								
e. Va	e. Various applications/smart objects								
f. Major Players/Industry, Standards.									
2. In dis	2. In discussion with the concerned faculty during Laboratory hours Student should plan the Mini project and prepare								
syno	psis								
3. The j	progress of work ar	nd discussion mu	ist be document	ted.					
4. Testi	4. Testing of final product, Preparation, Checking & Correcting be done in discussion with faculty								

5. The Student must submit a brief project report(25-30 pages) that must include the following a. Introduction

- b. Literature surveyc. Hardware & Software Requirements
- d. System Design Architecturee. Implementation (screenshots to be included)
- f. Testing
- g. Conclusion
- h. Future enhancements.
- j. Bibliography

Text Books								
1	FPGA Based Digital Design : Wayne Wolf, Pentice Hall, 2012							
2								
3								
4								
	References							
1	Digital System Design using VHDL, Charles H. Roth, PWS Publishing, a branch of							
	Thomson Learning							
2	Clive Maxfield, "The Design Warriors's Guide to FPGAs", Elsevier, 2004.							
3	Digital System Design using VHDL, Charles H. Roth, PWS Publishing, a branch of							
	Thomson Learning							
4	FPGA product catalog from Xilinx and Altera							

Useful Links										
1	https://nptel.ac.in/									
2	https://www.coursera.org/									
3 <u>https://forums.xilinx.com/</u>										
4										
CO-PO Mapping										
	Programme Outcomes (PO)									
	1	2	3	4	5	6				
CO1			2							
CO2	2									
CO3				2						
CO4			2			2				
The str Each C	The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High Each CO of the course must map to at least one PO.									

Assessment										
There are three components of lab assessment, LA1, LA2 and Lab ESE.										
IMP: Lab ESE is a separate head of passing. LA1, LA2 together is treated as In-Semester Evaluation.										
Assessmen	Based on	Based on Conducted by Typical Schedule (for 26-week Sem) M								
t				S						
TA1	Lab activities,	Lab Course	During Week 1 to Week 6	20						
LAI	attendance, journal	Faculty	Marks Submission at the end of Week 6	50						
LA2	Lab activities,	Lab Course	During Week 7 to Week 12	30						
	attendance, journal	Faculty	Marks Submission at the end of Week 12	50						

l

	Lab activities,	Lab Course	During Week	15 to Week 18		40		
Lade	ESE	attendance, journal	Faculty	Marks Submi	ssion at the end	of Week 18	40	
Week	1 indic	ates starting week of a	semester. The ty	pical schedule	of lab assessmer	nts is shown,		
conside	ering a	26-week semester. Th	e actual schedule	e shall be as per	academic calen	dar. Lab		
activiti	es/Lab	performance shall inc	lude performing	experiments, m	ini-project, pres	entations, drav	vings,	
prograi	mming	and other suitable act	ivities, as per the	nature and requ	irement of the l	ab course. The)	
experir	nental	lab shall have typicall	y 8-10 experimen	nts.				
_								
	Assessment Plan based on Bloom's Taxonomy Level (Marks) (For lab Courses)							
	Plan	m's Taxonomy I aval	T A 1	т л 2	Lob FSF	Total		

Assessment Plan based on Bloom's Taxonomy Level (Marks) (For lab Courses)									
Bloom's Taxonomy Level	LA1	LA2	Lab ESE	Total					
Remember									
Understand									
Apply	15			15					
Analyze	15	10		25					
Evaluate		10	20	30					
Create		10	20	30					
Total Marks	30	30	40	100					

Walchand College of Engineering, Sangli (Government Aided Autonomous Institute)								
	AY 2021-22							
			Course	Information				
Programme		M.'	Tech. (Electronics	Engineering)			
Class, Semest	er	Fir	st Year M.Tech., S	Sem I				
Course Code		5E	N552					
Course Name		Ac	tivity based lab E	mbedded Syste	em Design			
Desired Requ	isites:	Mi	croprocessors / Mi	crocontrollers				
		1						
Teaching Sc	heme]	Examination S	Scheme (Marks)			
Lecture	-	1	LA1	LA2	ESE	Total		
Tutorial	-		30	30	40	100		
Practical	2				Nil			
	Hrs/we	ek						
Interaction	-			C	redits: 1			
			Course	e Objectives				
1	To und	ersta	nd the Product De	velopment Pro	cess through Mini Project.			
2	To unde	ersta	nd budgeting throu	ıgh Mini proje	ct			
3	To use	Cor	tex M3 / M4 proce	essor architectu	re and its features			
4	To lear	n Al	RM Cortex –M Ar	chitecture and	Programming			
5	To und	ersta	nd the importance	of document d	lesign by compiling Technical	Report		
	on the I	Mini	Project work carri	ed out.				
	Course Outcomes (CO) with Bloom's Taxonomy Level							
At the end of t	he course	, the	students will be a	ble to,				
CO1	Identif	f y th	e requirements for	or the real wo	orld problems	Anal		

		vze
CO2	Understand and plan mini project based on ARM Cortex –M	Appl
		у
CO3	Design and build the project successfully	Desi
0.05		gn
	Deliver technical seminar based on the Mini Project work carried	Creat
CO4	out.	e

Guidelines for Mini Project

- 1. The students must understand following aspects while planning Mini Project a. Concept of ARM Cortex –M3/M4 programming
 - b. Importance
 - c. Interdisciplinary
 - d. Challenges
 - e. Various applications/smart objects
 - f. Major Players/Industry, Standards.
- 2. In discussion with the concerned faculty during Laboratory hours Student should plan the Mini project and prepare synopsis
- 3. The progress of work and discussion must be documented.
- 4. Testing of final product, Preparation, Checking & Correcting be done in discussion with faculty
- 5. The Student must submit a brief project report(25-30 pages) that must include the following a. Introduction
 - b. Literature survey
 - c. Hardware & Software Requirements
 - d. System Design Architecture
 - e. Implementation (screenshots to be included)
 - f. Testing
 - g. Conclusion
 - h. Future enhancements.
 - j. Bibliography

	Text Books							
1	Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2nd Edition							
2	Frank Vahid and Tony Givargis, "Embedded System Design", Wiley							
	References							
1	Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide:							
	Designing and Optimizing", Morgan Kaufman Publication							
2	Steve furber, "ARM System-on-Chip Architecture", Pearson Education							
3	Frank Vahid and Tony Givargis, "Embedded System Design", Wiley							

4	Technical references and user manuals on www.arm.com, NXP Semiconductor														
	www	www.nxp.com and Texas Instruments www.ti.com, ST Microelectronics www.st.com													
							Usef	ul Li	nks						
1							N	VPTE	EL Le	cture	S				
	CO-PO Mapping														
		Programme Outcomes (PO) PSO													
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	2														
CO2		2													
CO3			2	2											
CO4	CO4 2 2 2 1 1														
The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High															
			Eac	h CC) of th	ne co	urse r	nust	map 1	to at l	east (one P	О.		

	Assessment								
There are three components of lab assessment, LA1, LA2 and Lab ESE. IMP: Lab ESE is a separate head of passing. LA1, LA2 together is treated as In-Semester Evaluation.									
Assessmen	Based on	Conducted by	Typical Schedule (for 26-week Sem)	Mark					
t				s					
I A 1	Lab activities,	Lab Course	During Week 1 to Week 6	20					
LAI	LAI attendance, journal Faculty Marks Submission at the end of Week 6								
L A 2	Lab activities, Lab Course During Week 7 to Week 12								
LAZ	attendance, journal	Faculty	Marks Submission at the end of Week 12	50					
Lob ESE	Lab activities,	Lab Course	During Week 15 to Week 18	40					
Lauese	attendance, journal	Faculty	Marks Submission at the end of Week 18	40					
Week 1 indic	ates starting week of a	semester. The typ	pical schedule of lab assessments is shown,						
considering a	26-week semester. Th	ne actual schedule	shall be as per academic calendar. Lab						
activities/Lab performance shall include performing experiments, mini-project, presentations, drawings,									
programming	g and other suitable act	ivities, as per the	nature and requirement of the lab course. The	e					
experimental	lab shall have typicall	y 8-10 experimen	ts.						

Assessment Plan based on Bloom's Taxonomy Level (Marks) (For lab Courses)									
Bloom's Taxonomy Level	LA1	LA2	Lab ESE	Total					
Remember									
Understand									
Apply	15			15					
Analyze	15	10		25					
Evaluate		10	20	30					
Create		10	20	30					
Total Marks	30	30	40	100					

Walchand College of Engineering, Sangli						
(Government Aided Autonomous Institute)						
	AY 2021-22					
	Course Information					
Programme	M.Tech. (All Programs)					

Class, Sem	lester	Second Year M.Tech., Sem I						
Course Co	de	5EN553						
Course Na	me	Presentation and	Technical Re	eport Writing				
Desired R	equisites:							
Teachi	ng Scheme	Examination Scheme (Marks)						
Lecture	-	LA1	LA2	ESE	Total			
Tutorial	-	30	30	40	100			
Practical	-			Nil				
Interaction	n 1 Hrs/week			Credits: 1				
	· ·							
	Course Objectives							
1	Demonstrate th	he stages of the v	writing proce	ess (prewrite/draft/re	evise/edit) and apply			
1	them to techni	cal and workplac	e writing ta	sks.				
2	Produce docur	nents related to t	echnology a	nd writing in the wo	orkplace and will			
-	have improved	their ability to v	write clearly	, concisely, and acc	urately.			
3	Produce the ba	sic components	of letters, su	mmaries, descriptio	ns,process			
	explanations, p	proposals, and ot	her commor	forms of technical	writing.			
	Cour	rse Outcomes (CO	D) with Bloo	m's Taxonomy Leve				
At the end	of the course, the	e students will be a	able to,					
C01	Understand the	e use of variety of	of materials	to produce appropri	ate Understanding			
	technical/resea	arch reports						
CO2	202 Demonstrate the characteristics of technical and business writing Analyze							
CO3	Presentation of	f the report			Create			
			Guidelines					

- 1. Gather sources for the purpose of producing a research paper in a particular technical field;
- 2. Identify and use library resources (such as academic articles published in peer-reviewed journals) using the Internet, including catalogues, databases, indexes, bibliographies, and websites;
- 3. Adhere to guidelines for scholarly and unbiased sources.
- 4. Students will properly document sources and synthesize and integrate material from sources with their own ideas in research papers.
- 5. Documentation must be used in the course, according to the instructor's discretion.

	CO-PO Mapping														
	Programme Outcomes (PO) PSO														
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1					2										
CO2		3													
CO3		3													
CO4															
	The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High														
			Ea	ach CC	of the	course	e must	map to	o at lea	st one	PO.				

There are three	There are three components of lab assessment, LA1, LA2 and Lab ESE.									
IMP: Lab ESE is a separate head of passing. LA1, LA2 together is treated as In-Semester Evaluation.										
Assessmen	Based on	Based on Conducted by Typical Schedule (for 26-week Sem) Mat								
t				S						
ΤΑ1	Lab activities,	Lab Course	During Week 1 to Week 6	30						
LAI	attendance, journal	Faculty	Marks Submission at the end of Week 6							
1.4.2	Lab activities,	Lab Course	During Week 7 to Week 12	30						
	attendance, journal	Faculty	Marks Submission at the end of Week 12	50						
LabESE	Lab activities,	Lab Course	During Week 15 to Week 18	40						
Lau ESE	attendance, journal	Faculty	Marks Submission at the end of Week 18	40						

Week 1 indicates starting week of a semester. The typical schedule of lab assessments is shown, considering a 26-week semester. The actual schedule shall be as per academic calendar. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments.

Assessment Plan based	Assessment Plan based on Bloom's Taxonomy Level (Marks) (For lab Courses)										
Bloom's Taxonomy Level	LA1	LA2	Lab ESE	Total							
Remember											
Understand											
Apply	30	10		40							
Analyze		20	10	30							
Evaluate			10	10							
Create			20	20							
Total Marks	30	30	40	100							

Walchand College of Engineering, Sangli (Government Aided Autonomous Institute)								
	AY 2021-22							
	Course Information							
Programme		M.Tech. (Elect	ronics Engineeri	ing)				
Class, Semester		First Year M. T	Fech., Sem I					
Course Code		5EN554						
Course Name		Professional Skills 1						
Desired Requisites:	Desired Requisites:							
Teaching Sch	eme		Examination S	cheme (Marks)				
(Hrs)								
Lecture	-	LA1	LA2	ESE	Total			
Tutorial	-	30	30	40	100			
Practical	Practical -							
Interation	1		Cred	lits: 1				
	Course Objectives							

1	To provide a hands on experience of software in solving complex Electronics							
	engineering problems.							
2	To enhance the employability of Electronics engineering student.							
	Course Outcomes (CO) with Bloom's Taxonomy Level							
At t	At the end of the course, students will be able to,							
CO	Use of the software related to Electronics engineering effectively.	Evaluate						
1								
со	Develop the solution for Electronics engineering problem using	Create						
2	software.							
CO	Explain the process of problem solving using computing tools.	Understand						
3								
1								

Course Content

This course is based on computing as a tool to design and analyse the Electronics system. In the modern day work environment, the Electronics engineers should be able to simulate and solve complex problems on computers. The Electronics engineer must be highly computer literate. The engineer with strong fundamentals in Electronics Engineering and computer software proficiency is highly in demand from industry. Employability of the student can be enhanced by providing software training in Electronics engineering.

Text Books

1 Suitable books based on the software selected.

References

1 Suitable books based on the contents of software selected

Useful Links

1 As per the need of the software training

CO-PO Mapping										
		Programme Outcomes (PO)								
	1	2	3	4	5	6				
CO1	2									
CO2			2							
CO3		3				1				

•

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High Each CO of the course must map to at least one PO.

		Asses	SILLEIL						
There are three components of lab assessment, LA1, LA2 and Lab ESE.									
IMP: L	IMP: Lab ESE is a separate head of passing. LA1, LA2 together is treated as In-Semester								
Evaluat	tion.		-						
Asses	Based on	Conducted by	Typical Schedule (for 26-week	Mar					
smen			Sem)	ks					
t									
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 6 Marks Submission at the end of Week 6	30					
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 7 to Week 12 Marks Submission at the end of Week 12	30					

Lab ESE	Lab activities, attendance, journal	Lab Course Faculty	During Week 15 to Week 18 Marks Submission at the end of Week 18	40				
Week 1	indicates starting wee	ek of a semester. T	The typical schedule of lab assessments is	5				
shown,	considering a 26-weel	k semester. The ad	ctual schedule shall be as per academic					
calenda	calendar. Lab activities/Lab performance shall include performing experiments, mini-project,							
presentations, drawings, programming and other suitable activities, as per the nature and								
requirement of the lab course. The experimental lab shall have typically 8-10 experiments.								

Assessment Plan based on Bloom's Taxonomy Level (Marks) (For lab Courses)									
Bloom's Taxonomy Level	LA1	LA2	Lab ESE	Total					
Remember									
Understand	10	10	10	30					
Apply									
Analyze									
Evaluate	10	10	15	35					
Create	10	10	15	35					
Total Marks	30	30	40	100					

Walchand College of Engineering, Sangli										
(Government Aided Autonomous Institute)										
	AY 2021-22									
	Course Information									
Progra	mme		M.Tech. (Electronics	Engineering)						
Class, S	Semes	ter	First Year M.Tech., S	Sem I						
Course	e Code	;	5EN511							
Course	Nam	e	Professional Elective	1 -Advanced Digita	l Signal Processir	ıg				
Desired	d Requ	uisites:	Signals and Systems,	, Digital Signal Proce	essing					
Те	eachin	g Scheme	Ех	amination Scheme	(Marks)					
Lectur	e	3 Hrs/week	T1	T2	ESE	Total				
Tutoria	al	-	20	20	60	100				
Practic	al	-	Nil							
Interac	ction	-	Credits: 3							
			Course Ob	jectives						
1	To il	lustrate the conc	epts of Advanced Sigr	al Processing						
2	To ex	xplain the differe	ent techniques for desig	gn of filters and mult	irate systems					
3	To er	hable the student	s for the design and de	evelopment of Adapt	ive DSP systems					
	1.0	Course (Dutcomes (CO) with	Bloom's Taxonomy	Level					
At the e	end of	the course, the s	tudents will be able to	,		D:				
CU1 Explain the basic and advanced signal processing concepts 1 Design FIP and IIP filters with given specifications 1						Discuss				
CO2	Desiş		mers with given speci	neations		Solve				
CO3	Anal	yse the various a	lgorithms related with	multi-rate DSP		Analyz				

		e
CO4	Illustrate adaptive signal processing algorithms	Demon
04		strate

Modul	Module Contents	Hours
e		
I	Review of Digital Signal Processing Discrete Time Signals and systems, LTI Systems, Basic Signal Processing Operations, Discrete Time Systems-Classification, impulse and step responses, phase and group delays. Time domain and frequency domain characterization of LTI discrete time systems, Z Transform, Transfer function	8
	DSP Structures	
II	Block Diagram Representation, Equivalent Structures, Basic FIR Digital Filter Structures, Basic IIR Digital Filter Structures, All pass Filters, Tuneable IIR Digital Filters, IIR Tapped Cascaded Lattice Structures, FIR Cascaded Lattice Structures, Parallel All pass Realization of IIR Transfer Functions	6
	DFT Computation Techniques	
III	DFT-Definition and properties, symmetry properties, Circular convolution, Computation of DFT, Decimation in time (DIT) and Decimation in Frequency (DIF) Fast Fourier transform (FFT) algorithms, Linear filtering using FFT- overlap add, overlap save methods, Goertzel Algorithm	6
	Filter Design Technique	
IV	Bilinear Transformation Method of IIR Filter Design, Design of Low pass IIR Digital Filters, Design of High pass, Band pass and Band stop IIR Digital Filters, Spectral Transformations of IIR Filters, FIR Filter Design Based on Windowed series, Design of Digital Filters with Least-Mean-Square Error, Constrained Least- Square Design of FIR Digital Filters	8
	Multi-rate Signal Processing	
V	The Basic Sample Rate Alteration Devices, Filters in Sampling Rate Alteration Systems, Multistage Design of Decimator and Interpolator, The Poly phase Decomposition, Arbitrary-Rate Sampling Rate Converter, Digital Filters Banks, Two-Channel Quadrature-Mirror Filter bank	6
	Introduction to adaptive signal processing	
VI	Introduction to Adaptive Filters, Steepest descent technique, LMS algorithm- Convergence analysis, Learning curve, SVD	6

	Text Books							
	Sanjit K. Mitra, "Digital Signal Processing – A Computer based approach", Tata McGraw-Hill,							
1	4 th Edition, 2013							
2	Bernard Widrow, Samuel D. Stearns "Adaptive Signal Processing,", Prentice-Hall, Englewood							
	Cli, NJ, 1985							
	References							
1	J. G. Proakis, Dimitris K Manolakis, "Advanced Digital Signal Processing Principals,							
1	Algorithms and Applications,", Pearson,2007							
	Useful Links							
1	NPTEL Lectures							
	CO-PO Mapping							

		Programme Outcomes (PO)										PSO				
	1	2	3	4	5	6	7	8	9	10	11	12	1	l	2	3
CO1			2													
CO2						1										
CO3				2												
CO4																
The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High																
				Each	CO of	the co	ourse n	nust n	ap to	at leas	t one l	PO.				

Assessment Plan based on Bloom's Taxonomy Level (Marks) For Theory Course								
B	Bloom's Taxonomy Level	T1	T2	ESE	Total			
1	Remember							
2	Understand							
3	Apply	20	10	30				
4	Analyze		10	30				
5	Evaluate							
6	Create							
	Total	20	20	60	100			

Walchand College of Engineering, Sangli (Government Aided Autonomous Institute)									
	AY 2021-22								
		Cou	rse Informatio	n					
Program	ne	MTech. (Ele	ctronics engined	ering)					
Class, Ser	nester	First Year M	Tech., Sem II						
Course Co	ode	5EN512							
Course Na	ame	Professional	Elective 1 : Dig	gital VLSI Design					
Desired R	equisites:	Digital Techniques							
Teachir	ng Scheme	Examination Scheme (Marks)							
Lecture	3 Hrs/week	T1	T2	ESE	Total				
Tutorial	-	20	20	60	100				
Practical	-		· · · ·	Nil					
Interacti - Credits: 3									
on	on								
Course Objectives									

	Walchand College of Engineering, Sangli (Government Aided Autonomous Institute)	
1	To explain the relevance of CMOS technology in implementing digi	tal circuits
1	To explain the felevalee of envios technology in implementing dig	
	To discuss in details various logic styles (static, dynamic) in imp	blementing
2	CMOS circuits and the effect of choosing a particular style	on device
	performance from delay, power and area point of view.	
3	To develop the architectures of few data-path designs (system buildi	ng blocks)
	and an insight into extracting the functionality of displayed CMOS	circuit
4	To motivate the students to develop lifelong/self-learning attitude	
A. C. 1	Course Outcomes (CO) with Bloom's Taxonomy Level	
After the c	completion of the course the student should be able to	
	Apply the analytical expressions involving physical parameters,	Illustrate
CO1	process parameters and electrical parameters to characterize the	
	MOS transistors by taking into account the fundamental	
	principles involved with MOS devices	
GOA	Analyze static and dynamic CMOS circuits numerically to	Develop
CO2	compute the various device parameters and circuit performance	
	parameters_computational skills.	Analyza
CO3	compute the various device parameters and circuit performance	Anaryze
005	parameters	
	Select an appropriate logic style to design submicron MOS	Design
CO4	transistor based circuits using logical, analytical and	Design
	computational skills.	
	Design the self timed CMOS circuits and synchronous circuits	Dervelan
CO5	with built-in arbiters, synchronizers	Develop
CO5	with built-in arbiters, synchronizers	Develop
CO5 Module	Design the sen timed civros circuits, and synchronious circuits with built-in arbiters, synchronizers Module Contents	Hours
CO5 Module	Module Contents MOS Transistor	Hours
CO5 Module	Module Contents MOS Transistor MOS transistor theory, MOS under static conditions, Secondary	Hours 4
CO5 Module I	Module Contents MOS Transistor MOS transistor theory, MOS under static conditions, Secondary effects, Technology Scaling CMOS Insustant	Hours 4
CO5 Module I	Module Contents MOS Transistor MOS transistor theory, MOS under static conditions, Secondary effects, Technology Scaling CMOS Inverter CMOS inverter	Hours 4
CO5 Module I II	Module Contents MOS Transistor MOS transistor theory, MOS under static conditions, Secondary effects, Technology Scaling CMOS Inverter CMOS inverter, Static and Dynamic behaviour of CMOS inverter, Power and Energy-Delay. Impact of technology scaling on inverter	Hours 4 6
CO5 Module I II	Module Contents MOS Transistor MOS transistor theory, MOS under static conditions, Secondary effects, Technology Scaling CMOS Inverter CMOS inverter, Static and Dynamic behaviour of CMOS inverter, Power and Energy-Delay, Impact of technology scaling on inverter Combinational Static Logic Design	Hours 4 6
CO5 Module I II	Module Contents MOS Transistor MOS transistor theory, MOS under static conditions, Secondary effects, Technology Scaling CMOS Inverter CMOS inverter, Static and Dynamic behaviour of CMOS inverter, Power and Energy-Delay, Impact of technology scaling on inverter Combinational Static Logic Design Combinational static logic designs in CMOS, CMOS (Inverter and	Hours 4 6
CO5 Module I II III	Module Contents MOS Transistor MOS transistor theory, MOS under static conditions, Secondary effects, Technology Scaling CMOS Inverter CMOS inverter, Static and Dynamic behaviour of CMOS inverter, Power and Energy-Delay, Impact of technology scaling on inverter Combinational Static Logic Design Combinational static logic designs in CMOS, CMOS (Inverter and Complex gates), pseudo-nmos, pass-transistor logic, transmission	Hours 4 6 8
CO5 Module I II III	Module Contents MOS Transistor MOS transistor theory, MOS under static conditions, Secondary effects, Technology Scaling CMOS Inverter CMOS inverter, Static and Dynamic behaviour of CMOS inverter, Power and Energy-Delay, Impact of technology scaling on inverter Combinational Static Logic Design Combinational static logic designs in CMOS, CMOS (Inverter and Complex gates), pseudo-nmos, pass-transistor logic, transmission gate logic and design aspects for optimizing the performance	Hours 4 6 8
CO5 Module I II III	Module Contents MOS Transistor MOS transistor theory, MOS under static conditions, Secondary effects, Technology Scaling CMOS Inverter CMOS inverter, Static and Dynamic behaviour of CMOS inverter, Power and Energy-Delay, Impact of technology scaling on inverter Combinational Static Logic Design Combinational static logic designs in CMOS, CMOS (Inverter and Complex gates), pseudo-nmos, pass-transistor logic, transmission gate logic and design aspects for optimizing the performance Combinational Dynamic Logic Design	Hours 4 6 8
CO5 Module I II III	Module Contents MOS Transistor MOS transistor theory, MOS under static conditions, Secondary effects, Technology Scaling CMOS Inverter CMOS inverter, Static and Dynamic behaviour of CMOS inverter, Power and Energy-Delay, Impact of technology scaling on inverter Combinational Static Logic Design Combinational static logic designs in CMOS, CMOS (Inverter and Complex gates), pseudo-nmos, pass-transistor logic, transmission gate logic and design aspects for optimizing the performance Combinational Dynamic Logic Design Combinational dynamic logic designs using pre-charge evaluate	Hours 4 6 8
CO5 Module I II III IV	Module Contents MOS Transistor MOS transistor theory, MOS under static conditions, Secondary effects, Technology Scaling CMOS Inverter CMOS inverter, Static and Dynamic behaviour of CMOS inverter, Power and Energy-Delay, Impact of technology scaling on inverter Combinational Static Logic Design Combinational static logic designs in CMOS, CMOS (Inverter and Complex gates), pseudo-nmos, pass-transistor logic, transmission gate logic and design aspects for optimizing the performance Combinational Dynamic Logic Design Combinational dynamic logic designs using pre-charge evaluate logic, domino logic, np-CMOS logic , design aspects for	Hours 4 6 8
CO5 Module I II III IV	Module Contents MOS Transistor MOS transistor theory, MOS under static conditions, Secondary effects, Technology Scaling CMOS Inverter CMOS inverter, Static and Dynamic behaviour of CMOS inverter, Power and Energy-Delay, Impact of technology scaling on inverter Combinational Static Logic Design Combinational static logic designs in CMOS, CMOS (Inverter and Complex gates), pseudo-nmos, pass-transistor logic, transmission gate logic and design aspects for optimizing the performance Combinational dynamic logic designs using pre-charge evaluate logic, domino logic, np-CMOS logic , design aspects for optimizing the performance	Hours 4 6 8
CO5 Module I II III IV	Module Contents MOS Transistor MOS transistor theory, MOS under static conditions, Secondary effects, Technology Scaling CMOS Inverter CMOS inverter, Static and Dynamic behaviour of CMOS inverter, Power and Energy-Delay, Impact of technology scaling on inverter Combinational Static Logic Design Combinational static logic designs in CMOS, CMOS (Inverter and Complex gates), pseudo-nmos, pass-transistor logic, transmission gate logic and design aspects for optimizing the performance Combinational Dynamic Logic Design Combinational dynamic logic designs using pre-charge evaluate logic, domino logic, np-CMOS logic , design aspects for optimizing the performance, Comparison of static and dynamic designs	Hours 4 6 8
CO5 Module I II III IV	Module Contents MOS Transistor MOS transistor theory, MOS under static conditions, Secondary effects, Technology Scaling CMOS Inverter CMOS inverter, Static and Dynamic behaviour of CMOS inverter, Power and Energy-Delay, Impact of technology scaling on inverter Combinational Static Logic Design Combinational static logic designs in CMOS, CMOS (Inverter and Complex gates), pseudo-nmos, pass-transistor logic, transmission gate logic and design aspects for optimizing the performance Combinational Dynamic Logic Design Combinational dynamic logic designs using pre-charge evaluate logic, domino logic, np-CMOS logic , design aspects for optimizing the performance, Comparison of static and dynamic designs Sequential Logic Design	Hours 4 6 8
CO5 Module I II III IV V	Module Contents MOS Transistor MOS transistor theory, MOS under static conditions, Secondary effects, Technology Scaling CMOS Inverter CMOS inverter, Static and Dynamic behaviour of CMOS inverter, Power and Energy-Delay, Impact of technology scaling on inverter Combinational Static Logic Design Combinational static logic designs in CMOS, CMOS (Inverter and Complex gates), pseudo-nmos, pass-transistor logic, transmission gate logic and design aspects for optimizing the performance Combinational Dynamic Logic Design Combinational dynamic logic designs using pre-charge evaluate logic, domino logic, np-CMOS logic , design aspects for optimizing the performance, Comparison of static and dynamic designs Sequential Logic Design Timing metrics of sequential circuits. Sequential logic designs in	Hours 4 6 8
CO5 Module I II III IV V	Module Contents MOS Transistor MOS transistor theory, MOS under static conditions, Secondary effects, Technology Scaling CMOS Inverter CMOS inverter, Static and Dynamic behaviour of CMOS inverter, Power and Energy-Delay, Impact of technology scaling on inverter Combinational Static Logic Design Combinational static logic designs in CMOS, CMOS (Inverter and Complex gates), pseudo-nmos, pass-transistor logic, transmission gate logic and design aspects for optimizing the performance Combinational Dynamic Logic Design Combinational dynamic logic designs using pre-charge evaluate logic, domino logic, np-CMOS logic , design aspects for optimizing the performance, Comparison of static and dynamic designs Sequential Logic Design Timing metrics of sequential circuits, Sequential logic designs in CMOS. Static and dynamic latches and registers	Hours 4 6 8 8
CO5 Module I II III IV V	Module Contents MOS Transistor MOS transistor theory, MOS under static conditions, Secondary effects, Technology Scaling CMOS Inverter CMOS inverter, Static and Dynamic behaviour of CMOS inverter, Power and Energy-Delay, Impact of technology scaling on inverter Combinational Static Logic Design Combinational static logic designs in CMOS, CMOS (Inverter and Complex gates), pseudo-nmos, pass-transistor logic, transmission gate logic and design aspects for optimizing the performance Combinational Dynamic Logic Design Combinational dynamic logic designs using pre-charge evaluate logic, domino logic, np-CMOS logic , design aspects for optimizing the performance Sequential Logic Design Timing metrics of sequential circuits, Sequential logic designs in CMOS, Static and dynamic latches and registers Timing Issues in Digital Circuits	Hours 4 6 8 8
CO5 Module I II III IV V	Module Contents MOS Transistor MOS transistor theory, MOS under static conditions, Secondary effects, Technology Scaling CMOS Inverter CMOS inverter, Static and Dynamic behaviour of CMOS inverter, Power and Energy-Delay, Impact of technology scaling on inverter Combinational Static Logic Design Combinational static logic designs in CMOS, CMOS (Inverter and Complex gates), pseudo-nmos, pass-transistor logic, transmission gate logic and design aspects for optimizing the performance Combinational dynamic Logic Design Combinational dynamic logic designs using pre-charge evaluate logic, domino logic, np-CMOS logic , design aspects for optimizing the performance, Comparison of static and dynamic designs Sequential Logic Design Timing metrics of sequential circuits, Sequential logic designs in CMOS, Static and dynamic latches and registers Timing Issues in Digital Circuits Timing Classification, Synchronous Design (Clock skew, Jitter,	Hours 4 6 8 8
CO5 Module I II III IV V VI	Module Contents MOS Transistor MOS transistor theory, MOS under static conditions, Secondary effects, Technology Scaling CMOS Inverter CMOS inverter, Static and Dynamic behaviour of CMOS inverter, Power and Energy-Delay, Impact of technology scaling on inverter Combinational Static Logic Design Combinational static logic designs in CMOS, CMOS (Inverter and Complex gates), pseudo-nmos, pass-transistor logic, transmission gate logic and design aspects for optimizing the performance Combinational Dynamic Logic Design Combinational dynamic logic designs using pre-charge evaluate logic, domino logic, np-CMOS logic , design aspects for optimizing the performance, Comparison of static and dynamic designs Sequential Logic Design Timing metrics of sequential circuits, Sequential logic designs in CMOS, Static and dynamic latches and registers Timing Issues in Digital Circuits Timing Classification, Synchronous Design (Clock skew, Jitter, Clock Distribution), Self-Timed Circuits Design, Synchronizers	Hours 4 6 8 8 8

	Text Books															
		1	. Jan	M. R	abaey,	, Anan	tha Cl	nandra	kasan,	Boriv	voje Ni	ikolic,	"Digit	tal Int	egrate	d
1	Circuits, A System Perspective", Pearson Education, Second Edition, First															
1			Ind	lian Re	eprint,	2003.										
	2 Neil Weste, Kamran Eshraghian "Principles of CMOS VLSI Design" Addison															
2			2. 11		.s.c, K	annan	We	slev/P	earson	i Educ	cation.	2010		sign ;	, Auu	5011
											,					
								Refer	ences							
1	Ka	mran	Eshrag	ghian,	Puckn	ell an	d Eshi	raghia	n " <i>Ess</i>	ential	s of V	LSI C	ircuits	and S	System	s", ,
1	Pre	entice-	Hall (l	India),	2008											
	Su	ng-Mc	o Kang	, Yusı	ıf Leb	lebici	"СМС	OS Dig	ital In	tegrat	ted Cir	cuits:	Analy	vsis ar	ıd Des	ign",
2	Mc	Graw	Hill E	ducati	ion (In	dia), T	Third H	Edition	, 2003	3						
2	Na	:1 Was	ta D			Avon	Domoni	aa "C	MOGI	71 С1 Т) a ni a mi	" Dee	maan E	ducat	ion 20	00
3	INC	II Wes	ste, Da		arris, i	Ayanı	Danerj		I inko	LSIL	Jesign	, геа	ISOII E	uucai	1011, 20	00
1								IPTEI	LIIIKS	irec						
1							CO	-PO N	/appi	ng						
					Pr	ogran	ıme C	outcon	nes (P	0)					PSO	
		1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
C	01				2											
C	02						1									
C	03						1									
C	04			2												
C	05			- 1												
				-			2									
U	00						2									
		The s	trength	n of m	apping	g is to l	be wri	tten as	1,2,3	; Whe	re, 1:L	.ow, 2	Mediu	m, 3:	High	
				Ea	ach CO	O of th	e cour	se mu	st map	to at	least o	ne PO).			

	Assessment Plan based on Bloom's Taxonomy Level (Marks) For Theory Course								
E	Bloom's Taxonomy Level	T1	T2	ESE	Total				
1	Remember								
2	Understand								
3	Apply	20	10	30	60				
4	Analyze		10	30	40				
5	Evaluate								
6	Create								
	Total 20 20 60 100								

		Walchand Coll	ege of Engineering,	Sangli						
	(Government Aided Autonomous Institute)									
		A	AY 2021-22							
	Course Information									
Programme		M.Tech. (Electroni	cs Engineering)							
Class, Semest	ter	First Year MTech.,	Sem II							
Course Code		5EN513		1.5						
Course Name	<u>.</u>	Professional Electiv	ve 2-Biomedical Sign	al Processing						
Desired Requ	usites:	Signals and System	is, Digital Signal Proc	essing						
Teaching	Scheme		Examination So	heme (Marks)						
Lecture	3 Hrs/week	T1	T2	ESE	Total					
Tutorial	-	20	20	60	100					
Practical	_		N N	il						
Interaction	-		Cred	its: 3						
		Cou	ırse Objectives							
1	To study ori	gins and characterist	tics of some of the m	ost commonly used	biomedical signals					
-	including EC	CG, EEG, evoked pot	entials, and EMG							
2	To explore problems	application of estable	lished engineering m	ethods to complex	biomedical signals					
	Co	ourse Outcomes (CO	D) with Bloom's Tax	onomy Level						
After the com	pletion of the c	ourse the student sho	ould be able to							
CO1	Apply signal	processing techniqu	es to biomedical sign	als	Applying					
CO2	Analyze ECO points	G and EEG signal wi	th characteristic featu	re	Analyzing					
CO3	Model a bior	medical system			Creating					
	1				1					
Module		Modu	ule Contents		Hours					
	Introduction	n to Biomedical Sign	nals	·						
	Examples of	to Biomedical Signals	Objectives and difficult	10medical Signals,						
I	analysis.	7								
	Signal Conv									
	signals, Sig	nal conversion circu	uits. Application are	as of Bio -Signal						
	analysis – El	EG, ECG, Phonocard	liogram, Spiro Gram,	Evoked Signals						
	Signal Aver	aging and Data Cor	npression Technique	es filtar a truciaal						
п	averager sof	tware for signal aver	an averaging as a dig	signal averaging	6					
	Turning poi	nt algorithm, AZTE	EC algorithm, Fan al	gorithm, Huffman	, i i i i i i i i i i i i i i i i i i i					
	coding									
	Adaptive No	oise Cancellation								
	Adaptive int	erterence / Noise ca	ncellation: Types of i	noise in biosignals;						
III	Weiner filter	s - IIK allu FIK - NO rs - steenest descent	algorithm - I MS ag	lantive algorithm -	6					
	Adaptive no	bise canceller - can	cellation of 50 Hz	signal in ECG -						
	Cancellation	of maternal ECG in	foetal electrocardiogr	aphy						

IV	Cardiological signal processing Basic Electrocardiography, ECG data acquisition, ECG lead system, ECG signal characteristics (parameters and their estimation), Analog filters, ECG amplifier, and QRS detector, Power spectrum of the ECG, Bandpass filtering techniques, Differentiation techniques, Template matching techniques, A QRS detection algorithm, Realtime ECG processing algorithm, ECG interpretation, ST segment analyzer, Portable arrhythmia monitor.	7
V	Neurological signal processing Neurological signal processing: The brain and its potentials, The electrophysiological origin of brain waves, The EEG signal and its characteristics (EEG rhythms, waves, and transients), Correlation. Analysis of EEG channels: Detection of EEG rhythms, Template matching for EEG, spike and wave detection	6
VI	Modeling of Biomedical Systems Motor unit firing pattern, Cardiac rhythm, Formants and pitch of speech, Point process, Parametric system modeling, Autoregressive model, Autocorrelation method, Application to random signals, Computation of model parameters, Levinson-Durbin algorithm, Computation of gain factor, Covariance method, Spectral matching and parameterization, Model order selection, Relation between AR and Cepstral coefficients	8
	Text Books	
1	Reddy D C. "Modern Biomedical Signal Processing – Principles and Techn New Delhi, 2005	niques", TMH,
2	Eugene N. Bruce, "Biomedical Signal Processing and Signal Modeling", A Publication JOHN WILEY & SONS, INC	Wiley-Interscience
	References	
1	1. Akay M. "Biomedical Signal Processing", Academic press, Califo	rnia,1994.
2	Bronzino J D "The Biomedical Engineering handbook", CRC and Free pre	ss, Florida, 1995.
	Usoful Links	
1		
1	INFIEL LECTORES	

CO-PO Mapping																
	Programme Outcomes (PO) PSO															
	1	2	3	4	5	6	7	8	9	10	11	12	1		2	3
CO1			2													
CO2				2												
CO3						1										
CO4																
CO5																
CO6																
The strength of mapping is to be written as 1,2,3; Where, 1: Low, 2: Medium, 3: High																
Each CO	of the	course	e must	map t	o at lea	ast one	PO.									

	Assessment Plan based on Bloom's Taxonomy Level (Marks) For Theory Course									
B	Bloom's Taxonomy Level	T1	T2	ESE	Total					
1	Remember									
2	Understand									
3	Apply	20	10	30	60					
4	Analyze		10	30	40					
5	Evaluate									
6	Create									
	Total 20 20 60 100									

	Walchand College of Engineering, Sangli (Government Aided Autonomous Institute)					
	AY 2021-22					
	Course Information					
Programme	M.Tech. (Electronics Engineering)					
Class,	First Year M.Tech., Sem I					
Semester						
Course Code	5EN514					
Course Name	Professional Elective 2-Embedded Linux Programming					
Desired	Nil					
Requisites:						

Teaching Scheme	ļ	Exa	amination Scheme	e (Marks)				
Lecture	3 Hrs/week	T1	Total					
Tutorial	-	20	20	60	100			
Practical	-		N	il				
Interacti	-	Credits: 3						
on								

	Course Objectives								
1	To make students familiar with installation and use of the embedded Linux operating system								
2	To facilitate the students to learn the fundamentals of Linux as applied to embedded hardware								
3	To give exposure to system design using embedded Linux as per the industry trends								
	Course Outcomes (CO) with Bloom's Taxonomy Level								

At the en	d of the course, the students will be able to,	
CO1	Apply the understanding of Linux for Linux administration	Apply
CO2	Write, compile, debug multi-file, multi-threaded programs under Linux using utilities like make, gdb etc.	Write
CO3	Write programs for peripherals such as GPIO/Keyboard/LCD/Serial port, Programs for camera handling and signal processing for EL hardware	Design
CO4	Design external hardware for EL board such as Raspberry pi	Design

Modu	Module Contents	Hours
le		
I	Introduction Introduction to Linux, Linux Distributions, Open source Software, GPL, Facilities in Embedded Linux Boards used in Industry/Market, Important Accessories of Linux boards available/used in industry, Care to take in handling the Linux boards, Development Setup for EL, OS installation, init process, initrd, boot loaders, lilo and GRUB boot loaders, Case studies of Embedded Linux Based Systems	5
п	Linux file system and commands Linux File System, Permissions, CLI and Linux Shells, Linux Commands, Linux concepts, Shell Script, Basic Linux system administration tasks on the RPi. Linux commands for file and process management. Linux Programming, Multi-file C programming Using make utility, Makefile, GNU debugger. Transferring Files Between Systems, Kernel, building kernel image	б
III	Multithreading and Hardware Access Threads and processes, Multithreaded C programming. EL hardware design issues, Logic-level translation circuitry. Case studies of hardware of frequently used interfaces, Communication with EL board through network, EL GPIO control using sysfs, wiringPi and python. Python libraries	7
IV	Hardware Interfacing and Programming-I Using onboard I2C, SPI, and UART capabilities. Circuits to the RPi that interface to its I2C bus, Linux I2C-tools. Communicate between UART devices using both Linux tools and custom C or Python code. Interface to a low-cost GPS sensor using a UART connection. Extend the input/output capability using external serial ADCs, DACs, Increase the number of available GPIOs on the RPi using both I2C and SPI GPIO expanders	7

	Hardware Interfacing and Programming-II	
V	Using Interrupt functionality on devices. Increasing the number of available serial UART devices on the RPi using low-cost USB-to-TTL devices. USB Bluetooth adapter for the RPi and connect to it from a mobile device for the purpose of building a basic remote-control application. Using Wi-Fi and Xigbee along with EL board. Hardware design for given system specifications	7
VI	Basic Image Processing on Embedded Linux Camera interfacing to EL board, Capture image and video. Stream video data to the Internet using Linux applications and UDP, multicast, and RTP streams. Using OpenCV to perform basic image processing on the RPi. Use OpenCV to perform a computer vision face-detection task. Play audio data on the using HDMI audio and USB audio adapters	7

	Text Books															
	Christopher Hallinan, " <i>Embedded Linux Primer: A Practical Real-World Approach</i> ", Prentice Hall; 1 st															
	ed1	tion (S	Septem	ber 28	, 2006) Asttless	, ISBN	978-0	13/01	/836 Due au		~" W:	lasu De	مت الم	:	2000	
1	K10 Fol	$\frac{1}{1}$	stones,		Aattnev	V, Beg	ginning For D	g Linux oginno	Progra	ammin	g , W1	ley; Fo	ourth ed	ition (2008)	
	Ka	rim Y	aro, 'aghme	ur Io	n Mas	ters (Gilad I	Sen-Yo	nssef	Philinr	e Geri	ım "	Ruildin	o Eml	hedded	Linux
	Systems", O'Reilly Media; Second Edition (August 22, 2008) ISBN: 978-0596529680															
	Systems , O Kelliy Media; Second Edition (August 22, 2008) ISBN: 978-0596529680															
2	2 Richard Stones, Neil Matthew, " <i>Beginning Linux Programming</i> ", Wiley; Fourth edition (2008)															
	Felix Alvaro, "LINUX: Easy Linux For Beginners", Amazon.com															
3		Karin	n Yagh	mour,	Jon M	asters,	Gilad I	Ben-Yo	ossef, P	hilipp	e Gerur	n, <i>''Bu</i>	ilding I	Embed	ded Lin	ux
			System.	s", O'ŀ	Reilly N	Aedia;	Second	d Editio	on (Aug	gust 22	2, 2008)	ISBN	: 978-0	59652	9680	
-								Refe	rences							
	P. 1	Ragha	van. A	mol L	ad. Sri	ram N	eelakaı	ıdan. '	'Emhea	dded L	inux Sı	vstem	Design	and D)evelon	ment".
	Au	erbach	Publi	cations	; 1 edit	tion (D	ecemb	er 21, 2	2005), 1	ISBN:	978-08	49340	581		eretopi	,,
1	<u>htt</u>	p://cra	shcour	se.ca/ii	ntroduc	tion-L	inux-ke	ernel-p	rogram	ming-	2nd-edi	tion				
	<u>htt</u>	p://cra	shcour	se.ca/ii	ntroduc	tion-L	inux-ke	ernel-p	rogram	ming-	2nd-edi	tion				
2																
								Usefu	l Link	s						
1								NPTE	L Lect	ures						
							С	O-PO	Mapp	ing						
					F	rogra	mme (Outcon	nes (PC))					PSO	
		1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
C	01			2												
C	02				2											
C	03						1									
C	04															
		7	he stre	ength c	1 of mapr	ing is	to be w	ritten :	1 as 1.2 ?	l 3: Whe	re. 1:L	$\frac{1}{2}$ w. $2 \cdot 1$	1 Medium	1. 3:Hi	gh	
		-			Each	CO of	the co	urse m	ust ma	n to at	least or	1e PO		.,	0	
						2001				r to at						

	Assessment Plan based on Bloom's Taxonomy Level (Marks) For Theory Course												
B	Bloom's Taxonomy Level	T1	T2	ESE	Total								
1	Remember												
2	Understand												
3	Apply	20	10	30	60								
4	Analyze		10	30	40								
5	Evaluate												
6	Create												
	Total	20	20	60	100								

	Walchand College of Engineering, Sangli (Government Aided Autonomous Institute)											
AY 2021-22												
Course Information												
Programme		M. Tech. (Electr	onics Engineerin	g)								
Class, Semester	•	First Year M. Te	ch., Sem I									
Course Code		5IC502										
Course Name		Constitution of I	ndia									
Desired Requis	ites:											
Teaching	Scheme	Examination Scheme (Marks)										
Lecture	2	T1	T2	ESE	Total							
	<u> </u>											
	Hrs/week											
Tutorial	Hrs/week	20	20	60	100							
Tutorial Practical	Hrs/week	20	20	60	100							
Tutorial Practical Interaction	Hrs/week	20	20 Cred	60 its: Nil	100							
Tutorial Practical Interaction	Hrs/week	20 Course	20 Cred Objectives	60 its: Nil	100							
Tutorial Practical Interaction 1 To revie	Hrs/week - - - w and create av	20 Course wareness on variou	20 Cred Objectives as provisions in t	60 its: Nil he constitution of I	100 ndia.							
Tutorial Practical Interaction 1 To revie	Hrs/week - - w and create av Course O	20 Course wareness on variou utcomes (CO) with	20 Cred Objectives as provisions in the th Bloom's Tax	60 its: Nil he constitution of I onomy Level	100 ndia.							

CO1	Explain t	he premises informing the twin themes of liberty and freedom from a	understan					
	civil right	ts perspective.	d					
CO2	constitution emergence	onal role and entitlement to civil and economic rights as well as the e of nationhood in the early years of Indian nationalism	d					
CO3	Address t Revolutio Constituti	he role of socialism in India after the commencement of the Bolshevik on in 1917 and its impact on the initial drafting of the Indian ion	understan d					
Modu	le	Module Contents	Hours					
Ι	Histor (Com	y of Making of the Indian Constitution Drafting Committee,	4					
II	Pream	sophy of the Indian Constitution : ble Salient Feature	4					
III	Conto Funda Exploi Right Funda	burs of Constitutional Rights: mental Rights; Right to Equality; Right to Freedom; Right against itation; Right to Freedom of Religion; Cultural and Educational Rights; to Constitutional Remedies; Directive Principles of State Policy; mental Duties.	5					
IV	Organ Parlian Functi Appoi	ns of Governance: ment, Composition, Qualifications and Disqualifications, Powers and ions, Executive, President, Governor, Council of Ministers Judiciary, ntment and Transfer of Judges, Qualifications, Powers and Functions	5					
V	Local District Introd Corpo and t Organ Electe	Appointment and Transfer of Judges, Qualifications, Powers and Functions Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO ZilaPachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and American of Science met democracy						
VI	Electi Election and I Functi Institu	on Commission: on Commission: Role and Functioning. Chief Election Commissioner Election Commissioners. State Election Commission: Role and ioning. tte and Bodies for the welfare of SC/ST/OBC and women.	5					
		Toyt Pooks						
1	Dr. S	N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution 1st Edition	n. 2015.					
+	2	M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014						
	3	D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 201	5					
		References						
	1	The Constitution of India, 1950 (Bare Act), Government Publica	ation					
		Useful Links						
۱	1	https://en.wikipedia.org/wiki/Constituent_Assembly_of_Indi	a					
	1 2	https://en.wikipedia.org/wiki/Constituent_Assembly_of_Indi https://nptel.ac.in/courses/129/106/129106003/	a					
	1 2 3	https://en.wikipedia.org/wiki/Constituent_Assembly_of_Indi https://nptel.ac.in/courses/129/106/129106003/ https://nptel.ac.in/noc/courses/noc20/SEM2/noc20-1w02/	a					

CO-PO Mapping
Programme Outcomes (PO)

	1	2	3	4	5	6						
CO1			1									
CO2	2											
CO3				1		2						
	The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High											
		Each CO of the	course must ma	p to at least one	PO.							

I	Assessment Plan based on Blo	oom's Taxonom	y Level (Marks)) For Theory Co	ourse
Bloo	om's Taxonomy Level	T1	T2	ESE	Total
1	Remember				
2	Understand	20	20	60	100
3	3 Apply				
4	Analyze				
5	Evaluate				
6	Create				
	Total	20	20	60	100

		V	Valchand Co (Governm	ollege of Enginee ent Aided Autonomous I	ring, Sangli								
	AY 2021-22												
Course Information													
Programme M. Tech. (Electronics Engineering)													
Class,	Semes	ster	First Year M.	Fech., Semester II									
Course	e Code	e	5EN521										
Course	e Nam	e	RTOS based sy	ystem Design									
Desire	d Req	uisites:	Embedded Sys	stem Design									
Те	eachin	g Scheme	Examination Scheme (Marks)										
Lectur	e	3Hrs/week	T1	T2	ESE	Total							
Tutori	al	-	20	20	60	100							
Practio	cal	-											
Intera	ctio	-		Credits: 3									
n													
				Course Objectives									
1	To ill	lustrate Real Ti	me operating sys	stem with multi-taskin	g								
2	To ill	lustrate task syr	chronization of	various tasks									
3	To de	evelop student i	n latest Buses Li	ke USB, Ethernet									

4	To develop student to design GUI Applications									
	Course Outcomes (CO) with Bloom's Taxonomy Level									
At the	end of the course, the students will be able to,									
CO1	Illustrate RTOS concepts and multitasking to embedded systems	Understa nd								
CO2	Design RTOS based systems with Process Synchronization using semaphore, mutex, flags, messages etc.	Apply								
CO3	Explain Advanced multi-core processing systems and inter processor communication.	Apply								
CO4	Design embedded GUI based system, API for USB	Create								
CO5	O5 Create embedded system using various IO peripheral									
Modu	Module Module Contents									
Ι	RTOS Programming:- Need and Requirements of RTOS, Concept of Multitasking, Priority inversion, RTOS structure, TCB block design, Repetitive Timer Requirement, Memory Requirement for each Task	6								
Π	RTOS Process Synchronization:- System events and interrupts. Task I synchronization with Flags, Semaphore, Mutex. Inter process communication with Messages queue/Mail Box Multicere processors:									
III	Multi core processors:- Programming on Multi core processors, inter-core communication, interrupts handling, software architecture for multi core processors.	7								
IV	GUI Programming:- Graphical Display Interface, Touch Screen Interface, Graphic Display drivers, GUI API calls for Windows, Dialogs programming, Designing Menu, Widgets programming for Textbox, Label, Combo box etc. Designing Application with GUI	7								
V	USB Programming:- USB 2.0 specifications, USB block diagram, Device, Host Interface, concept of endpoint, Data transfer on USB bus, Various USB data transfers, API for USB Host and Device Programming, Writing Application with USB Host and Device									
VI	Ethernet Programming & Embedded Application :-Motivation, Ethernet Interface, API for Ethernet Programming, Writing Server Application with Ethernet interface. Designing Server Application with GUI	6								
	Text Books									
1	The Real-Time Kernel by Micrium	1 1								
2	systems) by Jim Cooling	led								
3	Embedded Systems: Introduction to Arm [®] Cortex [™] -M Microcontrollers, Fifth Edition by Jonathan W Valvano	(Volume 1)								
	References									
1	http://www2.keil.com/mdk5/cmsis/									
$\frac{2}{2}$	User Guide and Reterence Guide of LPC 1768, STM32F7									
<u> </u>	www.usb.org > Developers > Documents									
4	nups://www.segger.com/									
	Lapful Linka									
1	bttps://www.edv.org/ https://www.udacity.com/									
$\frac{1}{2}$	https://www.coursera.org/https://www.kerpel.org/									
$\frac{2}{3}$	https://community.arm.com/									
	<u>https://conintentry.arm.com/</u>									

CO-PO Mapping														
	Programme Outcomes (PO) PSO													
1	1 2 3 4 5 6 7 8 9 10 11 12											1	2	3

CO1			2												
CO2			2												
CO3			2												
CO4				2											
CO5				2		2							1	1	
The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High															
Each CO	of the c	ourse	must m	nan to a	at least	one PO).								

Assessment Plan based on Bloom's Taxonomy Level (Marks) For Theory Course								
Bloom's Taxo	T1	T2	ESE	Total				
1	Remember							
2	Understand	10	5	10	25			
3	Apply	10	5	20	35			
4	Analyze							
5	Evaluate							
6	Create		10	30	40			
Tota	20	20	60	100				

Walchand College of Engineering, Sangli (Government Aided Autonomous Institute)									
AY 2021-22									
		Course	Information						
Programme	M. Tech.	(Electronics	Engineering)						
Class, Semester		First Year	M.Tech., Sem	II					
Course Code		5EN522							
Course Name		Wireless S	Sensor Network	ks and IoT					
Desired Requisites:		None							
Teaching Scheme			Ex	amination Schem	e (Marks)				
Lecture	3 H/W	T1	T2	ESE	Total				
Tutorial	-	20	20	60	100				
Practical	-		1	Nil					
Interaction	-			Credits: 3					
	·								
		Course	e Objectives						
1 To explain the Wireless S	ensor Netw	ork and its a	pplications						
2 To develop understanding	To develop understanding of the Sensor node architecture								
3 To understand WSN conr	nectivity wit	h Internet							

4	4 To compare various MAC protocols for Wireless Sensor Network						
5	5 To explain in a concise manner how the general Internet as well as Internet of Things work.						
Course O	Course Outcomes (CO) with Bloom's Taxonomy Level						
	At the end of the course, the students will be able to,						
CO1	Identify various challenges and applications of Wireless Sensor Network	Apply					
CO2	Develop knowledge about Wireless Sensor Network Architecture	Apply					
CO3	Investigate various MAC protocols for Wireless Sensor Networks	Analyze					
CO4	Explore and learn about Internet of Things and Cloud	Apply					

Module	Module Contents	Hours				
	Module 1 : Introduction of WSN					
Ι	Overview of Wireless Sensor Networks, Applications and Challenges, Mobile ad	4				
	hoc networks and wireless sensor networks					
	Module 2 Wireless Sensor Node Architecture					
II	Hardware components, Energy consumption, Operating systems and execution	5				
	environments, examples of sensor nodes					
	Module 3 Wireless Sensor Network Architecture					
III	Types of sources and sinks, Optimization Goals and Figures of Merit, Design	5				
	Communication WSN Tunnaling					
	Module: 4 WSN (Medium access control)					
	Fundamentals of MAC protocols - I ow duty cycle protocols and wakeup					
IV	concepts Contention Based protocols Schedule-based protocols - SMAC –	5				
1 4	BMAC Traffic-adaptive medium access protocol (TRAMA) The IEEE 802 15 4	5				
	MAC protocol.					
	Module 5 IoT					
X /	IoT definitions: overview, applications, potential & challenges, and architecture.					
V	M2M Protocols for Sensor Networks. IoT CASE Study.	5				
	Module 6 Cloud and SDN					
VI	Introduction to Cloud Computing including benefits, challenges, and risks Cloud					
V1	Computing Models. SDN: Introduce software defined networking: the	4				
	background, the development, and the challenges.					
	Text Books					
1	Kazem Sohraby, Daniel Minoli, Taieb Znati, "Wireless Sensor Networks Technology	Protocols and				
	Applications", John Wiley & Sons Inc. Publication ,2007					
2	"Internet of Things Applications and Protocols", Wiely publication 2nd Ed.					
	References					
	Edgar H. Callaway, Jr. and Edgar H. Callaway, "Wireless Sensor Networks: Architect	ures and Protocols"				
1	CRC Press August 2003					
	, one i 1000, i 10500 2000					
2	Akyildiz, Mehmet Can Vuran,"Wireless Sensor Networks", John Wiley & Sons Ltd. 2	010				
2						
3	William Stallings "Foundations of Modern Networking : SDN, NFV, QoE, IoT and Cl	oud" Pearson				
	Education					
	Useful Links					
1	https://nptel.ac.in/noc/courses/noc18/SEM1/noc18-cs09/					
2	https://onlinecourses.nptel.ac.in/noc21_cs17/preview					

CO-PO Mapping															
	Programme Outcomes (PO) PSO														
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1			2	3											
CO2				1		3									
CO3			3			2									
CO4				2		2									
The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High															
			Each	CO	of the	e cou	rse m	nust n	nap to	o at le	east o	ne P	О.		

Assessment Plan based on Bloom's Taxonomy Level (Marks) For Theory Course									
Bloom's	Taxonomy Level	T1	T2	ESE	Total				
1	Remember								
2	Understand								
3	Apply	20	20	30	70				
4	Analyze			30	30				
5	Evaluate								
6	Create								
	Total	20	20	60	100				

Walchand College of Engineering, Sangli						
	(Government Aided Autonomous Institute)					
	AY 2021-22					
	Course Information					
Programme	M. Tech. (Electronics Engineering)					
Class, Semester	Class, Semester First Year M. Tech., Semester II					

Cours	e Code	9	5EN571									
Cours	e Nam	e	Activity based lal	b RTOS based syster	n Design							
Desire	d Req	uisites:	Embedded Syste	Embedded System Design								
Te	eaching	g Scheme	T 4.4	eme (Marks)								
Lectur	re	-		LA2	ESE	Total						
Tutor Droati		-	30	30	40	100						
Pracu Intoro	cal otio	2 Hrs/week		Cradita	. 1							
n	cuo	-		Creuits	1							
			Cours	e Obiectives								
1	To ur	nderstand the Pr	oduct Developme	nt Process through M	ini Project.							
2	To ur	nderstand budge	ting through Mini	project	5							
3	To de	esign RTOS bas	ed systems									
4	To le	arn GUI based	system design		1							
5	Tour	nderstand the in	portance of docur	nent design by compi	ling Technical Report on	the						
	Mini	Project work ca	$\frac{1}{2}$	with Dloom's Toyon	amy Laval							
At the	end of	the course the	students will be at	vitii biooni s raxon de to								
	Desig	n RTOS based	systems with Proc	ess Synchronization u	using semaphore, mutex	Appl						
CO1	, flag	s, messages etc.	~) ~		8F,	y						
CO2	Expl	ain Advanced	l multi-core pr	ocessing systems	and inter processor	Appl						
	comn	nunication.				у						
CO3	Desig	gn embedded G	UI based system, A	API for USB		Creat						
CO4	Crea	te embedded sy	stem using variou	s IO peripheral		Creat e						
	<u> </u>		Guidelines	for Mini Project								
1	The	tudente must u	derstand followin	a aspects while plann	ing Mini Project							
1.		incept of RTOS	based system	g aspects while plain	ing winn Project							
	b. Im	portance	e ase a system									
	c. Int	erdisciplinary										
	d. Ch	allenges										
	e. Va	rious applicatio	ns/smart objects									
	1. IVI8	yor rayers/ind	usury, standards.									
2.	In dis	scussion with th	e concerned facult	ty during Laboratory	hours Student should pla	n the						
	Mini	project and pre	pare synopsis		Ĩ							
3.	The p	progress of worl	k and discussion m	nust be documented.								
4.	Testi facul	ng of final prod ty	uct, Preparation, C	Checking & Correctin	g be done in discussion v	vith						
5.	The S follov a. Int b. Lit	Student must su wing roduction terature survey	bmit a brief projec	et report(25-30 pages)	that must include the							
	c. Ha	rdware & Softv	vare Requirements									
	d. Sy	stem Design Ar	chitecture									

- e. Implementation (screenshots to be included)f. Testingg. Conclusionh. Future enhancements.j. Bibliography

Text Books								
1	The Real-Time Kernel by Micrium							
2	Real-time Operating Systems: Book 1 - The Theory (The engineering of real-time embedded systems) by Jim Cooling							
3	3 Embedded Systems: Introduction to Arm® Cortex TM -M Microcontrollers, Fifth Edition (Volume 1) by Jonathan W Valvano							
	References							
1	http://www2.keil.com/mdk5/cmsis/							
2	User Guide and Reference Guide of LPC 1768, STM32F7							
3	www.usb.org > Developers > Documents							
4	https://www.segger.com/							
	Useful Links							
1	https://www.edx.org/ https://www.udacity.com/							
2	https://www.coursera.org/ https://www.kernel.org/							
3	https://community.arm.com/							

CO-PO Mapping															
		Programme Outcomes (PO) PSO													
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1			2												
CO2			2												
CO3			2												
CO4				2											
CO5				2		2							1	1	
The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High															
Each CO	of the c	course	must n	nap to a	at least	one PO).								

Assessment								
There are three	There are three components of lab assessment, LA1, LA2 and Lab ESE.							
IMP: Lab ES	E is a separate head of	passing. LA1, LA	A2 together is treated as In-Semester Evaluat	ion.				
Assessmen	Based on	Conducted by	Typical Schedule (for 26-week Sem)	Mark				
t				s				
ΤΑΊ	Lab activities,	Lab Course	During Week 1 to Week 6	20				
LAI	attendance, journal	Faculty	Marks Submission at the end of Week 6	50				
LAC	Lab activities,	Lab Course	During Week 7 to Week 12	20				
LAZ	attendance, journal	Faculty	Marks Submission at the end of Week 12	50				
Lob ESE	Lab activities,	Lab Course	During Week 15 to Week 18	40				
Lab ESEattendance, journalFacultyMarks Submission at the end of Week 18								
Week 1 indicates starting week of a semester. The typical schedule of lab assessments is shown,								
considering a	26-week semester. Th	ne actual schedule	shall be as per academic calendar. Lab					

activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments.

Assessment Plan based on Bloom's Taxonomy Level (Marks) (For lab Courses)									
Bloom's Taxonomy Level	LA1	LA2	Lab ESE	Total					
Remember									
Understand									
Apply	15			15					
Analyze	15	10		25					
Evaluate		10	20	30					
Create		10	20	30					
Total Marks	30	30	40	100					

Walchand College of Engineering, Sangli						
(Government Aided Autonomous Institute)						
AY 2021-22						
Course Information						
Programme	M.Tech. (Electronics Engineering)					
Class, Semester	First Year M.Tech., Sem II					
Course Code	5EN572					
Course Name	Activity based lab Wireless Sensor Networks and IoT					
Desired Requisites:	None					

Teaching Scheme	Examination Scheme (Marks)				
Lecture	-	LA1	LA2	ESE	Total
Tutorial	-	30	30	40	100
Practical	NT'1				
2 Hrs/week	N11				
Interaction	-	Credits: 1			

Course Objectives					
1	1 To understand the Product Development Process through Mini Project.				
2	To understand budgeting through Mini project				
3	To use Wireless Sensor Network protocols				
4	4 To learn IoT sensors interfacing				
5 To understand the importance of document design by compiling Technical Report on the Mini Project work carried out.					
Course Outcomes (CO) with Bloom's Taxonomy Level				
	At the end of the course, the students will be able to,				
CO1	Identify various challenges and applications of Wireless Sensor Network	Apply			
CO2	Develop knowledge about Wireless Sensor Network Architecture	Apply			
CO3	Investigate various MAC protocols for Wireless Sensor Networks	Analyze			
CO4	Explore and learn about Internet of Things and Cloud	Apply			
	Med Decise 4 Contractor				
	Mini Project Guideline				

- 6. The students must understand following aspects while planning Mini Project a. Concept of WSN and IoT
 - b. Importance
 - c. Interdisciplinary
 - d. Challenges
 - e. Various applications/smart objects
 - f. Major Players/Industry, Standards.
- 7. In discussion with the concerned faculty during Laboratory hours Student should plan the Mini project and prepare synopsis
- 8. The progress of work and discussion must be documented.
- 9. Testing of final product, Preparation, Checking & Correcting be done in discussion with faculty
- 10. The Student must submit a brief project report(25-30 pages) that must include the following a. Introduction
 - b. Literature survey
 - c. Hardware & Software Requirements
 - d. System Design Architecture
 - e. Implementation (screenshots to be included)
 - f. Testing
 - g. Conclusion
 - h. Future enhancements.
 - j. Bibliography

Text Books
Kazem Sohraby, Daniel Minoli, Taieb Znati, "Wireless Sensor Networks Technology
Protocols and Applications", John Wiley & Sons Inc. Publication ,2007
"Internet of Things Applications and Protocols", Wiely publication 2nd Ed.
References
Edgar H. Callaway, Jr. and Edgar H. Callaway, "Wireless Sensor Networks:
Architectures and Protocols", CRC Press, August 2003
Akyildiz, Mehmet Can Vuran,"Wireless Sensor Networks", John Wiley & Sons Ltd.
2010
William Stallings "Foundations of Modern Networking : SDN, NFV, QoE, IoT and
Cloud" Pearson Education
Useful Links
https://nptel.ac.in/noc/courses/noc18/SEM1/noc18-cs09/
https://onlinecourses.nptel.ac.in/noc21_cs17/preview

CO-PO Mapping	
Programme Outcomes (PO)	PSO

	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1			2	3											
CO2				1		3									
CO3			3			2									
CO4				2		2									
The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High Each CO of the course must map to at least one PO.															

Assessment							
There are three	There are three components of lab assessment, LA1, LA2 and Lab ESE.						
IMP: Lab ES	E is a separate head of	passing. LA1, LA	A2 together is treated as In-Semester				
Evaluation.	1	1	1	1			
Assessmen	Based on	Conducted by	Typical Schedule (for 26-week	Marks			
t			Sem)				
	I als activities	Lah Cauraa	During Week 1 to Week 6	1			
LA1	Lab activities,		Marks Submission at the end of	30			
	attendance, journal	Faculty	Week 6				
	I ab activition	Lab Course	During Week 7 to Week 12				
LA2	Lab activities,	Lab Course	Marks Submission at the end of	30			
	attendance, journal	Faculty	Week 12				
	Lab activities	Lab Course	During Week 15 to Week 18				
Lab ESE	Lau activities,		Marks Submission at the end of	40			
	attendance, journal	raculty	Week 18				

Week 1 indicates starting week of a semester. The typical schedule of lab assessments is shown, considering a 26-week semester. The actual schedule shall be as per academic calendar. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments.

Assessment Plan based on Bloom's Taxonomy Level (Marks) (For lab Courses)									
Bloom's Taxonomy Level	LA1	LA2	Lab ESE	Total					
Remember									
Understand									
Apply	15			15					
Analyze	15	10		25					
Evaluate		10	20	30					
Create		10	20	30					

Total Marks	30	30	40	100
-------------	----	----	----	-----

Walchand College of Engineering, Sangli									
AY 2021-22									
	Course Information								
Progra	amme		M.Tech. (Electronics	Engineering)					
Class,	Semes	ster	First Year M. Tech.,	Sem II					
Cours	e Code	e	5EN573						
Cours	e Nam	e	Industrial Project						
Desire	d Rea	uisites:							
	1								
Т	eachin	g Scheme		Examination Scheme	(Marks)				
Lectur	re	-	LA1	LA2	ESE	Total			
Tutori	ial		30	30	40	100			
Practi	cal				11				
Intera	ctio	1 Hr/Week		Credits: 1					
n									
		I							
			Course	Objectives					
1	To ui	nderstand indust	rial problems.						
2	To su	iggest engineeri	ng solutions to the defi	ned problem.					
3									
4		~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~			-				
At the	and of	Could the second the	rse Outcomes (CO) wi	th Bloom's Taxonomy	Level				
At the	Chos	e Formulate a c	elear problem	,		Apply			
CO1	Chos	e, i orindiate a e	near problem.			rippiy			
CO2	Selec	t and apply app	ropriate engineering me	ethods and tools for solv	ing the problem.	Create			
CO3	Deve	lop the project a	and its results following	g an established project n	nethodology.	Evaluat e			
CO4	Prese	ent the project re	sults.			Analyze			
			List of Experime	ents / Lab Activities					
Industrial Project: The Industry project will involve the selection of appropriate real time industry problem by understanding the working of particular industry application. Formulate the problem, select design and methodology to find the solution. Construct an electronic system by using appropriate hardware software tools. Each student should conceive, design and develop the idea leading to a project/product. The student should submit a soft bound report at the end of the semester. The final product as a result of Industry project should be demonstrated in phases at the time of examination. This will help student to understand structured management in industry , sustainable development, with consideration to both scientific and ethical aspects and its presentation with technical report.									
			Text	Books					
1	To be	e used based on	selected project						
2									

References						
1	1 Industry 4.0 : fourth Industrial Revolution guide to Industry 4.0					
2						
Useful Links						
1						
2						

CO-PO Mapping								
	Programme Outcomes (PO) PSO							PSO
	1	2	3	4	5	6		
CO1	3	2						
CO2				2		2	_	
CO3			2				_	
CO4		2					-	
The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High								
Each CO of the course must map to at least one PO.								

Assessment							
There are three components of lab assessment, LA1, LA2 and Lab ESE. IMP: Lab ESE is a separate head of passing. LA1, LA2 together is treated as In-Semester Evaluation							
Assessmen Based on Conducted by Typical Schedule							
t				s			
τ. Α 1	Lab activities,	Lab Course	During Week 1 to Week 6	20			
LAI	attendance, journal	Faculty	Marks Submission at the end of Week 6	50			
I A D	Lab activities,	Lab Course	During Week 7 to Week 12	30			
LAZ	attendance, journal	Faculty	Marks Submission at the end of Week 12	50			
Lob ESE	Lab activities,	Lab Course	During Week 15 to Week 18	40			
LauESE	attendance, journal	Faculty	Marks Submission at the end of Week 18	40			
Week 1 indic	ates starting week of a	semester. The typ	pical schedule of lab assessments is shown,				
considering a	26-week semester. Th	ne actual schedule	shall be as per academic calendar. Lab				
activities/Lab	performance shall inc	clude performing e	experiments, mini-project, presentations, drav	wings,			
programming	g and other suitable act	ivities, as per the	nature and requirement of the lab course. The	e			
experimental	lab shall have typicall	y 8-10 experimen	ts				

Assessment Plan based on Bloom's Taxonomy Level								
Bloom's Taxonomy Level	LA1	LA2	ESE	Total				
Remember								
Understand	30	10		40				
Apply		10	5	20				
Analyze		10	5	20				
Evaluate								
Create			30	30				
Total	30	30	40	100				

Walchand College of Engineering, Sangli (Government Aided Autonomous Institute)									
	AY 2021-22								
	Course Information								
Progr	amme		M. Tech. (Electroni	ics Engineering)					
Class,	Semester		First Year M. Tech	., Sem II					
Cours	e Code		5EN574						
Cours	e Name		Professional Skills	2					
Desire	ed Requisi	tes:							
			1						
	Teaching	Scheme		Examination Sche	eme (Marks)				
Lectu	re	-	LA1	LA2	ESE	Total			
Tutor	ial	-	30	30	40	100			
Practi	cal	-		<u> </u>		1			
Intera	ction	1 Hr/Week		Credits	1				
		1	1						
			Course C	Objectives					
1	1 To provide a hands on experience of software in solving complex Electronics Engineering problems								
2	2 To enhance the employability of Electronics Engineering student.								
		Course	Outcomes (CO) wit	h Bloom's Taxonor	ny Level				
At the	end of the	course, student	s will be able to,						
CO1	Use of th	ne software relat	ed to Electronics En	gineering effectively		Evaluate			
CO2	Develop	the solution for	Electronics Enginee	ring problem using s	oftware.	Create			
CO3	Explain t	the process of p	roblem solving using	computing tools.		Understand			
			2	a					
		<u> </u>	Course	Content					
the mo proble strong of the	ourse 1s ba odern day v ms on com fundamen student car	sed on compute work environme uputers. The Ele tals and compute n be enhanced b	ng as a tool to design ent, the Electronics E ectronics Engineer mu- ter software proficien by providing software	and analyse the Ele ngineer should be ab ust be highly compu- ncy is highly in dema training.	ctronics Engineering the to simulate and ster ter literate. The engine from industry. I	ng system. In solve complex gineer with Employability			
			Text]	Books					
1	Suita	ble books based	on the software sele	cted.					
			Refer	ences					
1	Suita	ble books based	on the contents of so	oftware selected					
			TT OT	T					
1	A a	or the need of the	Useful	Links					
1	As pe	er the need of th	e sonware training						

CO-PO Mapping										
	Programme Outcomes (PO)									
	1	2	3	4	5	6				
CO1	2									
CO2			2							
CO3		3				1				
The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High										
Each CO of the course must map to at least one PO.										

Assessment								
There are thre	There are three components of lab assessment, LA1, LA2 and Lab ESE.							
IMP: Lab ES	E is a separate head of	passing. LA1, LA	A2 together is treated as In-Semester Evaluation	ion.				
Assessmen	ssessmen Based on Conducted by Typical Schedule (for 26-week Sem)							
t				s				
τ. Α. 1	Lab activities,	Lab Course	During Week 1 to Week 6	30				
LAI	attendance, journal	Faculty	Marks Submission at the end of Week 6	50				
I A C	Lab activities,	Lab Course	During Week 7 to Week 12	20				
LAZ	attendance, journal	Faculty	Marks Submission at the end of Week 12	50				
LobESE	Lab activities,	Lab Course	During Week 15 to Week 18	40				
LauESE	attendance, journal	Faculty	Marks Submission at the end of Week 18	40				

Week 1 indicates starting week of a semester. The typical schedule of lab assessments is shown, considering a 26-week semester. The actual schedule shall be as per academic calendar. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments.

Assessment Plan based on Bloom's Taxonomy Level (Marks) (For lab Courses)								
Bloom's Taxonomy Level	LA1	LA2	Lab ESE	Total				
Remember								
Understand	10	10	10	30				
Apply								
Analyze								
Evaluate	10	10	15	35				
Create	10	10	15	35				
Total Marks	30	30	40	100				

Walchand College of Engineering, Sangli (Government Aided Autonomous Institute)						
		AY 2	2021-22			
		Course I	nformation			
Programme		M. Tech. (Electron	nics Engineering)			
Class, Seme	ster	First Year M. Tech	n., Semester II			
Course Code	e	5EN523				
Course Nam	ie	Professional Elective – 3 Image Processing and Pattern				
		Recognition				
Desired Req	uisites:	Signal Processing				
		1				
Teachin	g Scheme	Examination Scheme (Marks)				
ISE2	2 Hrs/week	T1	T2	ESE	Total	
10	-	20	20	60	100	
Practical	-					
Interaction	-		Credits	: 2		

	Course Objectives							
1	To imparts knowledge in the area of image and image processing							
2	To learn the fundamentals of Pattern recognition and to choose an appropriate	e						
-	feature							
3								
A1	Course Outcomes (CO) with Bloom's Taxonomy Level							
At the	end of the course, the students will be able to,							
CO1	filtering, segmentation and local features to solve image processing problems of real world application							
CO2	Apply image processing and pattern recognition techniques to detect Apply objects and activities in images	/						
CO3	Compare and parameterize different learning algorithms.for pattern Analy recognition	ze						
CO4								
Modu	le Module Contents							
	Fundamentals of Image Processing: Pixel brightness transformation,	5						
	position dependent brightness correction, gray scale transformation;							
	geometric transformation, local pre-processing image smoothening, edge							
Ι	detectors, zero-crossing, scale in image processing, canny edge detection,							
	parametric edge models, edges in multi spectral images, local pre-							
	processing and adaptive neighbourhood pre-processing; image							
	restoration							
	Image Segmentation: Threshold detection methods, optimal	3						
II	thresholding, multispectral thresholding, thresholding in hierarchical data							
	structures; edge based image segmentation- edge image thresholding,							
	edge relaxation, border tracing, border detection							
	Mathematical Morphology: Basic morphological concepts, four	5						
	morphological principles, binary dilation, erosion, Hit or miss							
111	transformation, opening and closing; thinning and skeleton algorithms;							
	Morphological segmentation –particles segmentation and watersneds,							
	Image Textures statistical texture description, mathods based on spatial	1						
	frequencies co. occurrence matrices edge frequency and texture	4						
IV	recognition method applications Image representation and description							
	representation boundary descriptors regional descriptors							
	Fundamentals of Pattern Recognition: Basic concents of pattern	1						
	recognition fundamental problems in pattern recognition system design	-						
V	concents and methodologies, example of automatic pattern recognition							
	systems, a simple automatic pattern recognition model							
	Pattern Classification Algorithms: Pattern classification by distance	5						
	function: Measures of similarity. Clustering criteria K means algorithm	-						
VI	Pattern classification by like hood function: Pattern classification as a							
	Statistical decision problem. Bayes classifier for normal patterns							
	Text Books							
1	Earl Gose and Richard Johnsonbaugh Steve Jost, "Pattern Recognition and	Image						
1	Analysis", PHI publication.	0						

2	Sing Tze Bow, M. Dekker, "Pattern Recognition and Image Processing", Springer, 1992
3	
	References
1	Rafael C. Gonzalez and Richard E. Woods, "Digital Image Processing", Addinson – Wesley.
2	M. A. SID – AHMED, "Image Processing Theory Algorithms and Architecture", McGraw Hill Inc.
3	
	Useful Links
1	https://www.coursera.org/
2	
3	
4	

CO-PO Mapping													
	Programme Outcomes (PO)												
	1	2	3	4	5	6							
CO1	3												
CO2			2										
CO3						2							
CO4													
The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High													

Each CO of the course must map to at least one PO.

Assessment

The assessment is based on 2 in-semester evaluations (ISE) of 10 marks each, 1 mid-sem examination (MSE) of 30 marks and 1 end-sem examination (ESE) of 50 marks.

MSE is based on the modules taught till MSE (typically Module 1-3) and ESE is based on all modules with 30-40% weightage on modules before MSE and 60-70% weightage on modules after MSE.

Assessment Plan based on Bloom's Taxonomy Level (Marks) For Theory Course								
B	Bloom's Taxonomy Level	T1	T2	ESE	Total			
1	Remember							
2	Understand	20	10		30			
3	Apply			30	30			
4	Analyze		10	30	40			
5	Evaluate							
6	Create							
	Total	20	20	60	100			

Walchand College of Engineering, Sangli	
(Government Aided Autonomous Institute)	

				AY 2021-2	2							
			Co	ourse Information	ation							
	Pro	gramme	M.Tech. (E	lectronics Eng	gineering)							
	Class,	Semester	First Year N	M.Tech., Sem	II							
	Cou	rse Code	5EN524									
	Cou	rse Name	Professiona	rofessional elective 3 - Analog VLSI Design								
De	esired	Requisites:	None									
T	'eachi	ng Scheme		Exami	nation Scheme (Marks)							
Lec	ture	-	T1	T2	ESE	Total						
Tute	orial	-	20	20 20 60 100								
Prac	tical	2 Hrs/week			Nil							
Inter	n - Credits: 2											
			C	ourse Object	ivas							
	Тое	xplain the analog	g circuit conc	epts based on	MOS devices in such a way to	develon in						
1	stud	ents	5 en eune cone	opis oused on		ae verop m						
	the i	nsight and intuit	ion towards N	AOS circuits								
2 To deliver the tips (or thumb rules) related with design of analog circuits throughout the												
	To motivate the students to develop lifelong/self-learning attitude through the individual											
3	task											
assignment												
Cour	se Ou	tcomes (CO) w	ith Bloom's I	Faxonomy Lo	evel							
		At th	e end of the c	ourse, the stu	dents will be able to,							
CO	Ana	lyze MOS devic	e circuits to d	erive the depe	endence of various electrical	Analyze						
$\frac{1}{\alpha}$	para	meters analytica	lly and graphi	ically.		T mary 20						
$\frac{co}{2}$	Dev	elop large signal	and small sig	transistors on	or single stage amplifiers and	Apply						
4	Desi	gn common sou	rce common	gate commo	n drain amplifier for given							
CO	spec	ifications. Furthe	er recognize t	heir application	on under various typical	Create						
3	situa	tions.										
со	Crit	icize the applica	tion of passiv	e and active c	urrent mirrors as constant							
4	curre	ent sources of re-	quired current	t value for mu	such circuits as loads	Apply						
	слрі	ani the propertie		ai pairs using	such cheuns as loads.							
Mod	ul		N	ladula Canta	nta	Houng						
e			10.	Iodule Conte	nts	Hours						
	1	Module 1:MOS	Device Physic	ics								
т		MOS transistor (Characteristics	s, Second Ord	er Effects, MOS device models	4						
1	(MOS device cap	bacitance, MC	JS small signa	al model) MOS model	4						
	1	Jarameters										
	1	Module 2:Single	e Stage Ampl	lifier Part I								
П	0	CS stage with res	sistance load,	diode connec	ted load, current source load,	6						
		CS stage with so	urce degenera	ation								
				11.01								
III	Module 3 :Single Stage Amplifier Part II5											

	source follower, common-gate stage, cascade stage, folded cascade, choice of device models									
	Module 4: Differential Amplifiers									
IV	Basic difference pair, differential mode response, common mode response, Differential pair with MOS loads	6								
	Module 5: Passive and Active Current mirrors									
	Basic current mirrors, Cascade mirrors, active current mirrors, Frequency Response:									
V	CS stage, Source follower, Common gate stage, Cascade stage and Difference pair.	7								
	Module 6:Operational Amplifiers									
VI	VI Design of 2-stage operational amplifier, gain boosting, Common mode feedback, Input range limitations, Slew rate, Power supply rejection ratio.									
	Text Books									
1	Behzard Razavi, Design of Analog CMOS Integrated Circuits, , TATA M Hill	cGraw-								
	Publication, Eight Edition onwards (2005)									
2										
	References									
1	R. Jacob Baker, CMOS, Circuit Design, Layout and Simulation, Wiley-Inter- (2008)	science,								
2	Allen, P.E. and Holberg, D.R., CMOS Analog Circuit Design, Oxford Univer (2002).	sity Press								
3	Web-sites: vlsi.expert.com, testbench.in, asic-world.com									
	Useful Links									
1	NPTEL Lectures									
2										

CO-PO Mapping																
	Programme Outcomes (PO)													PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3	
CO1			3	2									3			
CO2						3								3		
CO3			2			3							3			
CO4				3		2								3		

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High Each CO of the course must map to at least one PO.

Assessment

The assessment is based on 2 in-semester examinations in the form of T1 (Test-1) and T2 (Test-2) of 20 marks each. Also there shall be 1 End-Sem examination (ESE) of 60 marks. T1 shall be typically on modules 1 and 2, T2 based typically on modules 3, 4 and ESE shall be on all modules with nearly 50% weightage on modules 1 to 4 and 50% weightage on modules 5, 6.

Assessment Plan based on Bloom's Taxonomy Level (Marks) For Theory Course

	Bloom's Taxonomy Level	T1	T2	ESE	Total
1	Remember				
2	Understand				
3	Apply	20	10	30	60
4	Analyze			30	30
5	Evaluate				
6	Create		10		10
	Total	20	20	60	100

	Walchand College of Engineering, Sangli (Government Aided Autonomous Institute)												
			(Government Ai	ded Autonomous In	nstitute)								
			A	Y 2021-22									
D			Cours	se Information									
Progra	amm	2	M. Iech. (Electron	ics Engineering)									
Class,	Semo	ester	First Year M. Tech	n., Sem II									
Cours		1e	SEINS25	A. D. h. diana	1 A								
Cours	e Nar	ne i-i-i	Nil										
Desire	a ke	quisites:	1111										
Tracking Coloma													
Lootu		2 Hrs/wook			ESE	Total							
Tutor		2 1115/ WCCK	20	20	<u>60</u>	100							
Tutor Droati		00	100										
Intoro		tio											
n	icuo	-		Cre									
Course Objectives													
	To become familiar with basic principles of AI toward problem solving inference perception												
1	and	learning.	with Susie principies	of the container pro-	orem sorting, merenee, p	creeption,							
2	Тое	enlight the fundation	amentals of robotic s	systems.									
3	Тое	explain the basic	s of robot, robot Tra	nsformations and s	Sensors, Micro/Nano robo	tic systems.							
4		Com)	T1								
At the	end c	f the course the	students will be abl) WITH BIOOM'S I a	axonomy Level								
At the	Apr	ly basic princip	les of AI in solution	ns that require pro	blem solving, perception.	Apply							
CO1	kno	wledge represent	tation and learning										
CO2	Und	erstand the basic	c components of rob	ots and its applcati	ions	Understan							
CO3	Des	ign intelligent ro	bots using sensors.			Evaluate							
CO4		0 0											
Modu	le		Modu	ile Contents		Hours							
I		Artificial Intelli natural language systems. AI tech	gence : Introduction, processing, vision a niques- search know	Applications- Gan nd speech process ledge, abstraction.	mes, theorem proving, ing, robotics, expert	4							
П	Problem Solving: Problem Solving: II State space search; Production systems, search space control, depth-first, breadth-first search 8												

	Heuristic search - Hill climbing, best-first search, branch and bound. Problem Reduction, Constraint Satisfaction problems, Means-End Analysis. LA*							
	Algorithm, L-AO*Algorithm.							
III	 Knowledge Representation and Learning : Knowledge Representation issues, first order predicate calculus, Horn Clauses, Resolution, Semantic Nets, Frames, Partitioned Nets, Procedural Vs Declarative knowledge, Forward Vs Backward Reasoning. Learning: Concept of learning, learning automation, genetic algorithm, learning by inductions, neural nets. Handling uncertainties: Non-monotonic reasoning, Probabilistic reasoning, and Fuzzy logic. 	8						
IV	Robotics: Fundamentals of Robotics, Robot Kinematics: Position Analysis, Dynamic Analysis and Forces, Robot Programming languages & systems: Introduction, requirements of a robot programming language.	4						
	Robot Transformations and Sensors:							
v	 Robot kinematics-Types- 2D, 3D Transformation-Scaling, Rotation, Translation, Homogeneous coordinates, multiple transformation-Simple problems. Sensors in robot – Touch sensors-Tactile sensor – Proximity and range sensors – Robotic vision sensor-Force sensor, Light sensors, Pressure sensors. 							
	Robot cell Design and Micro/nano Robotics System:							
VI	Robot work cell design and control-Sequence control, Operator interface, Safety monitoring devices in Robot, Mobile robot working principle, Robot applications, Micro/ Nano robotics system overview, Biomimetic robot, Swarm robot Nano robot in targeted drug delivery system	8						
		1						
	Text Books							
1	Elaine Rich, Kevin Knight, Shivashankar B Nair, Artificial Intelligence, , Tata M Publishing Company Limited, Third edition 2009	AcGraw Hill						
2	N.J. Nilsson, "Principles of AI", Narosa Publ. House, 1990							
3	Craig. J. J. "Introduction to Robotics mechanics and control", Addison- Wesley, 1999.							
4								
	References							
1	Stuart Russell and Peter Norvig, Artificial Intelligence – A Modern Approach, Prentice Third Edition 2010	e Hall Series,						
2	S.R. Deb, Robotics Technology and flexible automation, Tata McGraw-Hill Educatio	n., 2009						
3	Groover M P, Industrial Robotics, Mc Graw Hill Ltd.							
4	Jazar, Theory of Applied Robotics, Springer							
	Useful Links							
1	https://www.coursera.org/							
2	https://nptel.ac.in/							
3								
4								

CO-PO Mapping														
				I	PSO									
	1	2	3	4	5	6								
CO1	3													
CO2			2											
CO3						2								
CO4														

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High Each CO of the course must map to at least one PO.

Assessment

	Assessment Plan based on Bloom's Taxonomy Level (Marks) For Theory Course												
B	Bloom's Taxonomy Level	T1	T2	ESE	Total								
1	Remember												
2	Understand	10	10	20	40								
3	Apply	10	10	20	40								
4	Analyze												
5	Evaluate			20	20								
6	Create												
	Total	20	20	60	100								

			Walchand Coll (Government A	lege of Engineering, ided Autonomous Ins	Sangli titute)							
				AY 2021-22	,							
			Cou	rse Information								
Progra	amme		M. Tech. (Electro	onics Engineering)								
Class,	Semes	ster	First Year M. Tech., Semester II									
Cours	e Code	е	5EN526									
Cours	e Nam	e	Professional Elec	tive 4-Embedded Lin	ux System Design							
Desired Requisites: Embedded Linux Programming												
Те	Teaching Scheme Examination Scheme (Marks)											
Lectur	re	2 Hrs/week	T1	T2	ESE	Total						
Tutor	ial	-	20	20	60	100						
Practi	cal	-										
Intera	ctio	-	Credits: 2									
n												
			Cou	urse Objectives								
1	To fa	cilitate students	s to learn the web t	echnology on embedd	led Linux platform.							
2	To he embe	elp the students	design static and d web framework.	lynamic website for so	olving social problems us	ing						
3	To he	elp the students	to write device dri	ver on embedded Lin	ux for controlling simple	hardware.						
	Course Outcomes (CO) with Bloom's Taxonomy Level											
At the	end of	the course, the	students will be ab	ole to,								
CO1	CO1 Design a website using a frontend, backend languages/ scripts and framework. Understan											

CO2	Connect embedded system with front end / back end using EL	Analyze					
CO3	Design and develop web based solution for social problems using the EL	Create					
CO4	Build a simple device driver for controlling hardware	Create					
Modu	e Module Contents	Hours					
Ι	Introduction to web technology: - Fundamentals of Web technology, Web server, Web Client, Server and client side scripting. Installation of Web server on EL boards and accessing them over intranet, Basics of HTML.	4					
п	Web Programming: - HTML and CSS, Using web server for static content, Responsive site basics, Bootstrap, Php scripting for server side programming, Handling hardware through php, python. Fundamentals of database, Database design techniques, Design of dynamic web content using PHP with interface to sensors and actuators	7					
III	to sensors and actuators Web Design Framework: - PHP Frameworks Code igniter, Helper, Libraries, Session, Process of online site hosting, Send email messages directly from the RPi and utilize them as a trigger for web services such as IFTTT. Integrating payment gateway for in FL based systems.						
IV	 Embedded Linux based System Design: - System Design based on Embedded Linux using Web Technology. Design for various online socially relevant systems. Systems engineering for online systems based on EL. System implementation using Raspberry Pi / Beagle Bord Linux Design Design design for demonstels. Kernel Decomposition for 						
v	Linux Device Driver:- Device driver fundamentals, Kernel Programming for Device driver design, Building the environment, Implementing the driver, Setting up the ports/Hardware, Compiling the driver, Loading the driver into the kernel, Using the driver, device driver programming						
VI	Applications: - Case study on embedded Linux system design for web based technology.	6					
1	Robin Nixon, <i>Learning PHP, MySQL & JavaScript</i> , O'Reilly publication, 4th Edition ISBN: 9789352130153	, 2015,					
2	Kogent Learning Solutions Inc, <i>Web Technologies: HTML, JAVASCRIPT, PHP</i> , Drea (2009) ISBN: 978-8177229974	mtech Press					
3	John Madieu, "Linux Device Drivers Development", Ed. 1 2017, ISBN: 97817852800)09					
	References						
1	"Embedded Linux Device drivers", https://lwn.net/Kernel/LDD3/						
2	<i>"Web Technology"</i> , https://www.geeksforgeeks.org/web-technology/#beginning						
3	Dr. Sudip Misra, NPTEL Course: "Introduction to Internet of Things", IIT Kharagpur https://onlinecourses.nptel.ac.in/noc17_cs22/preview	•					
1	Useful Links						
1	nttps://www.edx.org/						
2	nups://www.udacity.com/						
5	https://www.coursera.org/						
4	nups://www.kernel.org/						

CO-PO Mapping																
	Programme Outcomes (PO)													PSO		
	1 2 3 4 5 6 7 8 9 10 11 12											1	2	3		
CO1	2															
CO2	2															

CO3			2											
CO4				2								1	1	
The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High														
Each CO of the course must map to at least one PO.														

	Assessment Plan based on Bloom's Taxonomy Level (Marks) For Theory Course										
B	Bloom's Taxonomy Level	T1	T2	ESE	Total						
1	Remember										
2	Understand	10		20	30						
3	Apply	10	10	20	40						
4	Analyze										
5	Evaluate										
6	Create		10	20	30						
	Total	20	20	60	50						

	Walchand College of Engineering, Sangli (Government Aided Autonomous Institute)										
	AY 2021-22										
	Course Information										
Programme M.Tech. (Electronics Engineering)											
	Class,	Semester	First Year M.Tech	., Sem II							
	Cour	se Code	5EN575								
	Cour	so Nomo	Activity based Lal	o Professional Electi	ve 3 Image Process	sing and					
	Cour	se maine	Pattern Recognition Lab								
]	Desired	Requisites:	Digital Image Processing								
	Teachi	ng Scheme	Examination Scheme (Marks)								
Lec	ture	-	LA1	LA2	ESE	Total					
Tut	orial	-	30	30	40	100					
Prac	ctical	2 Hrs/week	Nil								
Inter	action	-	Credits: 1								
	Course Objectives										
1	To und	erstand the Produc	t Development Proc	ess through Mini Pro	ject.						
2	To und	erstand budgeting	through Mini projec	t							

3	To use Image Processing and Pattern Recognition Algorithms	
4	To understand the importance of document design by compiling Technical Report on the M	ini
-	Project work carried out.	
Cours	e Outcomes (CO) with Bloom's Taxonomy Level	
	At the end of the course, the students will be able to,	
	Describe different techniques used for image analysis	Unde
CO		rstan
1		ding
		A 1
CO	Apply both supervised and unsupervised clasification methods to detect and characterize	Appl
2	patterns in real-world data	yıng
CO	Implement simple pattern classifiers, classifier combinations, and structural pattern	Creat
	recognizers.	ing
3		
	Mini Project Guideline	
1.	The students must should learn following concepts before planning Mini Project	
	a. Basic point processing operations in MATLAB	
	b. Image Transformation Methods	
	c. Spatial Filtering on images	
	d. Edge detection algorithms	
	e. Morphological image processing algorithms and its applications	
	1. Object Detection Algorithms	
	g. Classification and Clustering Algorithms	
	n. Introduction to Computer vision Toolbox	
2.	In discussion with the concerned faculty during Laboratory hours Student should plan the N	Aini
2.	project and prepare synopsis	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,
	L Grand L L L L L C G C L L L	
3.	The progress of work and discussion must be documented.	
4.	Testing of final system, Preparation, Checking & Correcting be done in discussion with fac	ulty
_		
כ.	The Student must submit a brief project report (25-30 pages) that must include the following	g
	a. Introduction	
	o. Herduler sulvey	
	d. System Design Architecture	
	e Implementation (screenshots to be included)	
	f Testing	
	g Conclusion	
	h. Future enhancements.	
	j. Bibliography	
	Text Books	
1	Earl Gose and Richard Johnsonbaugh Steve Jost, "Pattern Recognition and Image Anal	ysis",
	Sing Tze Bow M. Dekker, "Pattern Recognition and Image Processing" Springer 100	12
2	Sing ize dow, w. Dekkei, rauem kecognition and image processing, springer, 199	·∠
	References	
1	Rafael C. Gonzalez and Richard E. Woods. "Digital Image Processing". Addinson – W	eslev
		j·

2	C.N	1.Bisho	op, "Pa	attern F	Recogn	ition &	& Machine Learning", Springer, 2006					
3												
Useful Links												
1	http	https://www.coursera.org/										
2												
3												
4												
						CO-l	PO Mapping					
				Pr	ogran	nme O	utcomes (PO)	PSO				
	1	2	3	4	5	6						
CO1	3											
CO2												
CO3				2		3						
The stren	The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High											
The streng	Each CO of the course must map to at least one PO.											

	Assessment									
There are three components of lab assessment, LA1, LA2 and Lab ESE.										
IMP: Lab ES	E is a separate head of	passing. LAI, LA	A2 together is treated as In-Semester Evaluat	ion.						
Assessmen	essmen Based on Conducted by Typical Schedule (for 26-week Sem) Mark									
t				S						
T A 1	Lab activities,	Lab Course	During Week 1 to Week 6	20						
LAI	attendance, journal	Faculty	Marks Submission at the end of Week 6	30						
LAC	Lab activities,	Lab Course	During Week 7 to Week 12	20						
LAZ	attendance, journal	Faculty	Marks Submission at the end of Week 12	50						
LobESE	Lab activities,	Lab Course	During Week 15 to Week 18	40						
	attendance, journal	Faculty	Marks Submission at the end of Week 18	40						
Week 1 indic	ates starting week of a	semester. The typ	pical schedule of lab assessments is shown,							
considering a	26-week semester. Th	ne actual schedule	shall be as per academic calendar. Lab							
activities/Lab	performance shall inc	lude performing of	experiments, mini-project, presentations, drav	wings,						
programming	g and other suitable act	ivities, as per the	nature and requirement of the lab course. The	e						
experimental	lab shall have typicall	y 8-10 experimen	ts.							

Assessment Plan based on Bloom's Taxonomy Level (Marks) (For lab Courses)										
Bloom's Taxonomy Level	LA1	LA2	Lab ESE	Total						
Remember										
Understand	15			15						
Apply	15	20	20	55						
Analyze										
Evaluate										
Create		10	20	30						
Total Marks	30	30	40	100						

	Walchand College of Engineering, Sangli									
				AY 2021-22	,					
Course Information										
	ProgrammeM.Tech. (Electronics Engineering)									
	Class, S	Semester	First Year M.	Fech., Sem II						
	Cours	se Code	5EN576							
	Cours	e Name	Activity based	l Lab Analog VLSI	Design					
Desired Requisites: None										
			·							
I	leachin	g Scheme		Examination	Scheme (Marks))				
Lec	ture	-	LA1	LA2	ESE	Τ	Total			
Tut	orial	-	30	30	40		100			
Prac	ctical	2 Hrs/week			Nil					
Inter	ractio n	-		Cr	edits: 1					
			1							
Course Objectives										
1	1 To understand the Product Development Process through Mini Project.									
2 To understand budgeting through Mini project										
3	3 To Cadence EDA tools for designing and simulating analog CMOS circuits									
4	To Cl 2-stsg	MOS analog cir ge Operational	rcuits and desig amplifier for gi	n single stage CS, ven specifications	CG, CD, differer	ntial amp	olifiers and			
5	To un Mini I	derstand the im Project work ca	portance of doc rried out.	ument design by co	ompiling Technica	l Report	on the			
Cour	se Out	comes (CO) wi	th Bloom's Tay	xonomy Level						
Cour	se out	At th	he end of the co	urse, the students v	vill be able to,					
CO 1	Analy drain bias u Cader	yze MOS transi current for des using nee EDA tools	istors by charac igning the phys	eterizing them for sical dimensions a	targeted value of nd the required ga	gm or ate	Analyze			
CO 2	Expla schen differ	ain and demons natic to symbol ential amplifier	strate the comp generation to s	lete flow of Cader simulation for CS,	ce tools from CG, CD and		Demonstr ate			
CO 3	Build Source schen entry expre	and evaluate b e Follower, Ca natic design for various loa ssions.	by simulating the second stage, directly distance of the stage of the stage of the second stage of the sec	he single stage am fferential pair etc.) e gain values with	plifier circuits (CS) using MOSFETs a theoretical	S, s	Evaluate			
CO 4	Desig gain a	n differential p nd UGB.	pair circuits wit	h active current m	irror load for give	en	Create			
Mod	ule		Moc	dule Contents			Hours			

11.	 The students must understand following aspects while planning Mini Project a. Concept of Cadence EDA tools for designing and simulating analog CMOS circuits b. CMOS analog circuits and design single stage CS, CG, CD, differential amplifiers and 2-stsge Operational amplifier for given specifications. c. To characterize the transistors for the voltage conditions seen by the circuit with goal of optimizing dimensions for given ID or trans-conductance. b. Importance c. Interdisciplinary d. Challenges e. Various applications/smart objects f. Major Players/Industry, Standards. In discussion with the concerned faculty during Laboratory hours Student should plan the Mini project and prepare synopsis The progress of work and discussion must be documented.
15.	The progress of work and discussion must be documented.
14.	Testing of final product, Preparation, Checking & Correcting be done in discussion with faculty
	 a. Infoduction b. Literature survey c. Hardware & Software Requirements d. System Design Architecture e. Implementation (screenshots to be included) f. Testing g. Conclusion h. Future enhancements. j. Bibliography
	Text Books
1	Behzard Razavi, Design of Analog CMOS Integrated Circuits, , TATA McGraw-Hill
	Publication, Eight Edition onwards (2005)
2	
	References
1	R. Jacob Baker, CMOS, Circuit Design, Layout and Simulation, Wiley-Inter- science, (2008)
2	Allen, P.E. and Holberg, D.R., CMOS Analog Circuit Design, Oxford University Press (2002).
3	Web-sites: vlsi.expert.com, testbench.in, asic-world.com
	Useful Links
1	NPTEL Lectures
2	

CO-PO Mapping															
	Programme Outcomes (PO)										P	80			
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1			3	2									3		
CO2						3								3	

CO3			2			3						3		
CO4				3		2							3	
The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High														
Each CO of the course must map to at least one PO.														

	Assessment Plan based on Bloom's Taxonomy Level (Marks) For Theory Course										
B	Bloom's Taxonomy Level	T1	T2	ESE	Total						
1	Remember										
2	Understand										
3	Apply	20	10	30	60						
4	Analyze			30	30						
5	Evaluate										
6	Create		10		10						
	Total	20	20	60	100						

Assessment Plan based of	Assessment Plan based on Bloom's Taxonomy Level (Marks) (For lab Courses)											
Bloom's Taxonomy Level	LA1	LA2	Total									
Remember												
Understand												
Apply	15		20	35								
Analyze	15	10	10	35								
Evaluate		10	10	20								
Create		10		10								
Total Marks	30	30	40	100								

Walchand College of Engineering, Sangli (Government Aided Autonomous Institute)											
	AY 2021-22										
Course Information											
Programme		M.Tech. (Electr	onics Engineerin	ıg)							
Class, Semester First Year M.Tech., Sem II											
Course Code 5EN577											
Course Name		Elective 4 -Acti	vity based lab Ro	obotics and Artific	ial Intelligence						
Desired Requisites:		None									
Teaching Scheme		Examination Scheme (Marks)									
Lecture		LA1	LA2	ESE	Total						
	-										
Tutorial	-	- 30 30 40 100									
Practical		Nil									
2 Hrs/week											

Interaction		-	Credits: 1						
			Course Objectives						
1	To use artificial intellig	gence	algorithms to design robot						
2	To understand the desig	gn Pro	ocess through Mini Project.						
3	To understand budgetin	g thr	ough Mini project						
4	To understand the importance of document design by compiling Technical Report on the Mini Project work carried out.								
	Course	e Out	tcomes (CO) with Bloom's Taxonomy Level						
At the end of the cou	urse, the students will be	able	to,						
CO1	Identify the component	nts to	o design robot for particular task	Apply					
CO2	Build the designed ap	plica	ition.	Create					
CO3	Test the project for different test cases Evaluate								
CO4	Present the work carr	ried o	but	Analyze					

Guidelines for Mini Project

- 6. The students must understand following aspects while planning Mini Project
 - a. Concept of algorithms to insert artificial intelligence.
 - b. Need of sensors, positioning in robotics
 - c. Problem identification
 - d. Design parameters in selection of components
 - e. Student should plan the Mini project and prepare synopsis in discussion with the concerned faculty
- 7. The progress of work and discussion must be documented.
- 8. Analysis and testing of intermediate steps of product
- 9. The Student must submit a brief project report(15-20 pages) that must include the following points
 - a. Introduction
 - b. Literature survey
 - c. Hardware & Software Requirements
 - d. System Design
 - e. Implementation (screenshots to be included)
 - f. Testing
 - g. Conclusion
 - h. Future enhancements.
 - j. Bibliography

Text Books										
1	Jain N, Artificial Intelligence: making a system intelligent, 2018, ISBN: 9788126579945									
2										
Reference	References									
1	J. Norberto Pires, Altino Loureiro and Gunnar Bölmsjo, _Welding Robots -									

	Tec 10:	Technology,System Issues and Applications_, Springer-Verlag 2006, ISBN-10:1852339535													
2	3. I Ma	Ben-Z	Cion S ry_, 2	Sandle Inded	er, _F . 1999	Robot: 9 by A	ics: I Acade	Design emic F	ning t Press,	he M ISBN	lechai V 0-12	nisms 2-618:	for 520-4	Autor	nated
Useful Links															
1	<u>htt</u>	https://nptel.ac.in/													
2	https://www.coursera.org/														
CO-PO Mapping															
		PO PSO													
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	3														
CO2			2												
CO3					2										
CO4															
The stree Each CC	ngth) of tl	of ma	pping urse n	g is to nust r	be w nap to	ritten 5 at le	as 1, east or	2,3; V ne PC	Where	, 1:Lo	ow, 2:	Medi	um, 3	3:Hig	1

	Assessment											
There are three components of lab assessment, LA1, LA2 and Lab ESE.												
IMP: Lab ESE is a separate head of passing. LA1, LA2 together is treated as In-Semester Evaluation.												
Assessmen	Based on	Conducted by	Typical Schedule (for 26-week Sem)	Mar								
t				ks								
LA1	Lab activities,	Lab Course	During Week 1 to Week 6	30								
LAI	attendance, journal	Faculty	Marks Submission at the end of Week 6									
LA2	Lab activities,	Lab Course	During Week 7 to Week 12	20								
	attendance, journal	Faculty	Marks Submission at the end of Week 12	50								
Lob ESE	Lab activities,	Lab Course	During Week 15 to Week 18	40								
Lab ESE	attendance, journal	Faculty	Marks Submission at the end of Week 18	40								
Week 1 indic	ates starting week of a	semester. The typ	pical schedule of lab assessments is shown,									
considering a	26-week semester. Th	ne actual schedule	shall be as per academic calendar. Lab									

activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments.

Assessment Plan based on Bloom's Taxonomy Level (Marks) (For lab Courses)											
Bloom's Taxonomy Level	LA1	LA2	Lab ESE	Total							
Remember											
Understand											
Apply	15			15							
Analyze	15	10		25							
Evaluate		10	20	30							
Create		10	20	30							
Total Marks	30	30	40	100							

	Walchand College of Engineering, Sangli (Government Aided Autonomous Institute)										
	AY 2021-22										
	Course Information										
	Prog	gramme	M.Tech. (Electroni	cs Engineering)							
	Class,	Semester	First Year M.Tech.	, Sem II							
	Cour	se Code	5EN578								
	Cour	se Name	Activity based lab	Professional Elective	4 Embedded Linux Sy	stem Design					
-	Desired	Requisites:	None								
	Teaching Scheme Examination Scheme (Marks)										
Lec	ture	-	LA1	LA2	ESE	Total					
Tut	orial	-	30	30	40	100					
Pra	ctical	2 Hrs/week		Nil							
Inter	action	-		Credits	:1						
Course Objectives											
1	1 To understand the Product Development Process through Mini Project.										
2	To und	erstand budgeting t	hrough Mini project								
3	To use	Embedded Linux									
4	To lear	n system Architec	ure, configuration ar	nd Programming							
5	To und	erstand the importa	nce of document des	ign by compiling Tech	nical Report on the M	ini Project					
-	work ca	arried out.									
Cours	e Outco	mes (CO) with Bl	oom's Taxonomy Lo	evel	1						
00	T 1 4 4	At t	he end of the course,	the students will be at	ble to,	A 1					
	Identi	iy the requirement	ts for the real work	a problems		Analyze					
	Under	stand and plan min	i project based on R	obotice and AI or Emb	edded Linux	Apply					
$\frac{1}{2}$	Under		i project based on R			rippiy					
CO	Design	and build the pro	ject successfully			Design					
<u> </u>	DP			· D · (1 ·	1 4	Create					
4	Delive	r technical semin	ar based on the Mi	ni Project work carri	ea out.	Create					
			Mini Proj	ect Guideline							

6.	The students must understand following aspects while planning Mini Project
	a. Concept of Front End and Back End Design, Web environment setup and integrating web technology
	with Linux based embedded system

- b. Importance
- c. Interdisciplinary
- d. Challenges
- e. Various applications/smart objects
- f. Major Players/Industry, Standards.
- 7. In discussion with the concerned faculty during Laboratory hours Student should plan the Mini project and prepare synopsis
- 8. The progress of work and discussion must be documented.
- 9. Testing of final product, Preparation, Checking & Correcting be done in discussion with faculty
- 10. The Student must submit a brief project report(25-30 pages) that must include the following a. Introduction
 - b. Literature survey
 - c. Hardware & Software Requirements
 - d. System Design Architecture
 - e. Implementation (screenshots to be included)
 - f. Testing
 - g. Conclusion
 - h. Future enhancements.
 - j. Bibliography

Text Books Robin Nixon, Learning PHP, MySQL & JavaScript, O'Reilly publication, 4th Edition, 2015, 1 ISBN: 9789352130153 Kogent Learning Solutions Inc, Web Technologies: HTML, JAVASCRIPT, PHP, Dreamtech Press 2 (2009) ISBN: 978-8177229974 3 John Madieu, "Linux Device Drivers Development", Ed. 1 2017, ISBN: 9781785280009 References "Embedded Linux Device drivers", https://lwn.net/Kernel/LDD3/ 1 2 "Web Technology", https://www.geeksforgeeks.org/web-technology/#beginning Dr. Sudip Misra, NPTEL Course: "Introduction to Internet of Things", IIT Kharagpur. 3 https://onlinecourses.nptel.ac.in/noc17_cs22/preview **Useful Links** https://www.edx.org/ 1 2 https://www.udacity.com/ 3 https://www.coursera.org/ 4 https://www.kernel.org/

	CO-PO Mapping														
		Programme Outcomes (PO) PSO													
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1			2	3											
CO2				1		3									
CO3			3			2									

CO4				2		2									
The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High															
Each CO of the course must map to at least one PO.															

Assessment											
There are three components of lab assessment, LA1, LA2 and Lab ESE.											
IMP: Lab ES	E is a separate head of	passing. LA1, LA	A2 together is treated as In-Semester Evaluat	ion.							
Assessmen	sessmenBased onConducted byTypical Schedule (for 26-week Sem)I										
t				S							
I A 1	Lab activities,	Lab Course	During Week 1 to Week 6	30							
LAI	attendance, journal	Faculty	Marks Submission at the end of Week 6	50							
I A D	Lab activities,	Lab Course	During Week 7 to Week 12	20							
LAZ	attendance, journal	Faculty	Marks Submission at the end of Week 12	30							
Lab ESE	Lab activities,	Lab Course	During Week 15 to Week 18	40							
	attendance, journal	Faculty	Marks Submission at the end of Week 18	40							
*** 1 4 1 11											

Week 1 indicates starting week of a semester. The typical schedule of lab assessments is shown, considering a 26-week semester. The actual schedule shall be as per academic calendar. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments.

Assessment Plan based on Bloom's Taxonomy Level (Marks) (For lab Courses)											
Bloom's Taxonomy Level	LA1	LA2	Lab ESE	Total							
Remember											
Understand											
Apply	15			15							
Analyze	15	10		25							
Evaluate		10	20	30							
Create		10	20	30							
Total Marks	30	30	40	100							

Wa	Walchand College of Engineering, Sangli (Government Aided Autonomous Institute)							
	AY 2021-22							
	Course Information							
Programme	M.Tech. (Electronics Engineering)							
Class, Semester	First Year M.Tech., Sem II							
Course Code	5OE108							

	Cours	ourse Name Open Elective - Introduction to Embedded Systems								
De	esired	Requisites:	None							
			1							
Т	'eachir	ng Scheme		Exa	mination Scheme (Mark	s)				
Lec	ture	2 Hrs/week	T1	T2	ESE	Tota	l			
Tute	orial	-	20	20	60	100				
Prac	ctical	-		1	Nil					
Inter	actio									
1	n	-			Credits: 2					
			1							
				Course Obje	ectives					
1	To in	troduce Embedo	ded Systems	and their app	lications					
1										
2	To de	To develop understanding about Microcontrollers								
3	To introduce hardware components of Embedded Systems									
4	Toex	To explain fundamentals of Arduino								
5	5 To explore Arduino based applications and programming									
Cour	se Out	comes (CO) wi	th Bloom's	Taxonomy L	.evel					
	At the end of the course, the students will be able to,									
CO 1	Unde	erstand Embedd	led Systems	and Identify	their applications		Apply			
CO 2	Deve	lop knowledge	about hardwa	are and softw	are of Embedded System	s	Apply			
CO 3	Anal	yze Arduino bas	sed systems a	and their prog	gramming		Analy			
CO 4	Expl	ore and learn A	rduino based	systems app	lications		Apply			
Modu	ule			Module Co	ntents		Hours			
	N	Aodule 1 Introd	luction							
		Embedded Syste	ms and gene	ral purpose c	omputer systems, history	,				
I	c	lassifications, ap	oplications an	nd purpose of	embedded systems Char	acteristics	4			
1	a	nd Applications	of embedde	d systems: op	erational and non-operati	onal	-			
	q	uality attributes	. Embedded	Systems App	lications-Application spe	cific –				
		Ashing machine	e, domain spe	cific - autom	lotive					
		Microprocessors	and microco	ntrollers RL	SC and CISC controllers	Big endian				
II	a	nd Little endian	processors.	Application s	pecific ICs. Programmab	le logic	5			
	d	evices, COTS, s	ensors and a	nsors and actuators, communication interface. embedded						
	fi	irmware, other s	ystem comp	onents.						
	N	Iodule 3 Embe	dded Hardv	vare						
	1	Memory map, i/	o map, interr	upt map, pro	cessor family, external pe	ripherals,	_			
III	n	nemory – RAM	, ROM, type	s of RAM an	d ROM, memory testing,	CRC	5			
	,l	Hash memory.	eripherals:	Control and	Status Registers, Device	Driver,				
		mer Driver - W	atchdog Timers							

	Module 4 Introduction to Arduino	
IV	Arduino device, Features of Arduino, Components of Arduino board, Description of Microcontrollers, Installation of Arduino IDE on Ubuntu Linux OS Run the arduino executable file, Using IDE to prepare Arduino sketch, Uploading and running the sketch, Program notation: variables, functions, control flow, Arduino conventions. The concept of a program variable. Numerical values and basic numerical operators. if/then/else Iteration using for loops. Real world timing and the delay() function	5
v	 Module 5 Input/Ouput Progrmming Sensor Inputs:- Definition, Types. Interfacing arduino to different sensors- light sensor, temperature sensor, humidity sensor, pressure sensor sound sensor, distance ranging sensor, water/detector sensor, smoke, gas, alcohol sensor, ultrasonic range finder Displays: Basics of LED's and LCD's. Interfacing arduino to LED's- blinking single LED, blinking multiple LED's, 7 segment display , traffic light ,LED flashes ,LED dot matrix ,pulsating lamp. Interfacing to LCD's- Basic LCD control, LCD temperature control, display a message on LCD screen, scrolling of text Touch screens, Reading and writing to SD card 	5
VI	Module 6 Arduino Applications Case studies : Arduino based robot car , Arduino based PLC, industrial application	4
	Text Books	
1	Shibu K V . "Introduction to embedded systems". Tata Mcgraw-Hill. 1 st edition	
2	"Arduino Cookbook."Michael Margolis	
	References	
1	"Embedded Systems", Rajkamal, Tata Mcgraw-Hill	
2	"Beginning Arduino", Michal Mc Roberts, Second Edition	
3	Michal Mc Roberts "Beginning Arduino" Second Edition, Technology in Action	
	Useful Links	
1	NPTEL Lectures	
2		

	CO-PO Mapping											
	Programme Outcomes (PO)										PSO	
1 2 3 4 5 6 7 8 9 10 11 12								1	2	3		

CO1			2								3		
CO2						3						3	
CO3			3			2					3		
CO4				2		2						3	
	The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High												

Each CO of the course must map to at least one PO.

Assessment

Assessment Plan based on Bloom's Taxonomy Level									
Bloom's Taxonomy Level	ISE1	MSE	ISE2	ESE	Total				
Remember									
Understand									
Apply	10	30		30	70				
Analyze			10	20	30				
Evaluate									
Create									
Total	10	30	10	50	100				

Walchand College of Engineering, Sangli (Government Aided Autonomous Institute)									
	AY 2021-22								
Course Information									
Programme M. Tech. (Electronics Engineering)									
Class, Semester	First Year N	M. Tech., Se	em II						
Course Code	5IC501								
Course Name	Value Education								
Desired Requisites:									
Teaching Sc	heme		Examination Scheme (Marks)						
Lecture	2 Hrs/wee	ek	T1	T2	E	Total			
					S				
					E				
Tutorial	-	-	20	20	6	100			
Dere effect					0				
Practical	-	-							

Intera	action			- Credits: 0						
				Course O	bjectives					
1	To impart	knowledge o	on value of e	ducation and	l self- develo	opment.				
2	To imbibe	good values	in students.							
3	To highlig	ht importanc	e of characte	er.						
		Cou	rse Outcom	es (CO) wit	h Bloom's T	Caxonomy L	evel			
At the	end of the c	ourse, stude	nts will be a	ble to,				TT 1 . 1		
CO 1	Explain va	lue of educa	tion and self	- developme	ent.			Understand		
 CO Summarize importance of good character, and Behaviour development. 2 							Evaluate			
N	Module Module Contents							Hours		
1		Values or	d calf dava	lonmont S	Pooial value	a and indi	vidual	110015		
	Ι	attitudes. Work ethics, Indian vision of humanism, Moral and non- moral valuation. Standards and principles, Value judgments.						6		
	Π	Importance reliance, c Honesty, I Love for n	6							
	IIIPersonality and Behaviour Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline, Punctuality, Love and Kindness, Avoid fault Thinking, Free from anger, Dignity of labour universal brotherhood and religious tolerance, True friendship, Happiness vs. suffering, love for truth, Aware of self- destructive habits, Association and Cooperation, Doing best for							7		
	IV	Character and Competence –Holy books vs. Blind faith, Self- management and Good health, science of reincarnation, Equality, Nonviolence, Humility, Role of Women, All religions and same message, Mind your Mind, Self-control. Honesty, Studying effectively						7		
				T (1						
	1	Chakrobor	ty, S.K. "Va Press New	alues and E	thics for org	ganizations [Theory	and practice", Oxford		
			11000, 1VCW							
				Refer	ences					
	1									
		·		Useful	Links					
	1	https://nim and-Legisl	suniversity.c	org/wp-conte lures.pdf	ent/uploads/2	2018/02/Val	ue-Eduo	cation-Human-Rights-		
	2	http://cbsea	academic.nic	c.in/web_ma	terial/Value	Edu/Value%	20Educ	cation%20Kits.pdf		
	3	https://ww	w.verywelln	nind.com/per	rsonality-dev	velopment-2	795425			
	4	https://trud	lreadz.com/2 hink-for-our	2019/09/10/b selves/	lind-faith-in	-religion-de	stroys-c	our-ability-to-		
			CO-PO Maj	oping						
		Pr	ogramme C	outcomes (P	0)					
	1	2	3	4	5	6				
CO 1	2				1	2				

CO	1		1			2	
2	1		1			2	
The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium,							
			3:High				
Each CO of the course must map to at least one PO.							

	Assessment Plan based on Bloom's Taxonomy Level (Marks) For Theory Course									
B	loom's Taxonomy Level	T1	T2	ESE	Total					
1	Remember									
2	Understand	10	10	30	50					
3	Apply									
4	Analyze									
5	Evaluate	10	10	30	50					
6	Create									
	Total	20	20	60	100					