Walchand College of Engineering, Sangli

(Government Aided Autonomous Institute)

AY 2023-24

Course Information

Programme	B. Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem.VII
Course Code	5EN401
Course Name	Power Electronics and Drives
Desired Requisites:	Basic Electrical Engineering, Circuit Theory

Teaching Scheme		Examination Scheme (Marks)			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
Practical	-				
Interaction	-	**Credits: 3**			

Course Objectives

1	**Explain** the working of modern power semiconductor devices and their applications.
2	**Explain** the working of power converter circuits like controlled rectifier, inverter, AC voltage controller and chopper and provide the knowledge of performance parameters of converters in the analysis of their performance.
3	**Explain** the use of different power control techniques like converters, choppers, inverters and cycloconverters to control the speed of DC motors and Induction motors.
4	**Illustrate** to choose an appropriate power electronic circuit and a power semiconductor device while designing an electrical power control system.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**Explain** the working of power semiconductor devices such as SCR, GTO, Power MOSFET and IGBT.	Understand
CO2	**Analyze** the performance of controlled rectifiers, DC to DC converters, Inverters, AC to AC converter.	Analyze
CO3	**Evaluate the** performance parameters of controlled rectifier, DC to DC converter, DC to AC converter and AC to AC converter.	Evaluate
CO4	**Analyze** the speed control techniques/ methods for AC and DC motors.	Analyze

Module	Module Contents	Hours
I	**Power Semiconductor Devices** SCR (Silicon Controlled Rectifier): two transistor model, protection circuits, series and parallel operation of SCR, triggering and commutation circuits; GTO, TRIAC, DIAC, Power Diode, Power BJT, Power MOSFET, IGBT.	7
II	**Phase Controlled Rectifiers** Single phase half and full wave controlled rectifier with R and RL load, Single phase half controlled (semiconverter) and fully controlled bridge rectifier. Three phase half wave controlled rectifier with resistive load, three phase half controlled and fully controlled bridge rectifier with R and RL load; Calculation of performance parameters of line commutated converters: Fourier analysis; effect of source impedance on the performance of controlled rectifiers.	9
III	**Inverters and AC voltage Controllers** Single phase half and full bridge inverter using transistor/MOSFET/IGBT, performance parameters, Fourier analysis of inverter output voltage; Three phase bridge inverter- 120^0 and 180^0 conduction mode; PWM inverters; Series and Parallel resonant inverter. AC voltage controllers: single phase and three phase AC voltage controllers; Cycloconverters: single phase to single phase, three phase to single phase, three phase to three phase cycloconverter.	8
IV	**DC to DC converters** Choppers: principles of operation, control strategies: TRC, current limit control; types of chopper, step up chopper, multiphase chopper; SMPS.	4

(SKP)

HOD ELN

V	**D.C. Motor Control** Equivalent circuit, speed torque characteristics (separately excited and series motor), operating modes, single phase and three phase controlled rectifier fed drives; four quadrant drive-single phase and three phase dual converter; Chopper-fed DC drive.	6
VI	**A.C. Motor Control** Equivalent circuit, speed torque characteristics, speed control methods-stator voltage control, rotor voltage control, frequency control, stator voltage and frequency control (V/F); Vector Control.	6

	Text Books
1	M. D. Singh & K. B. Khanchandani, "*Power Electronics*", Second Edition, Tata McGraw-Hill Publishing Company Ltd., New Delhi, 2007.
2	M.H. Rashid, "*Power Electronics: Circuits, Devices & Applications*", Third Edition, PHI, New Delhi, 2008.
3	P. S. Bimbhra, "*Power Electronics*", Third Edition, Khanna Publishers, 2004.
4	

	References
1	P. C. Sen, "*Power Electronics*", First Edition, Tata McGraw Hill Publishing Company Ltd, 2008.
2	V. R. Moorthi, "*Power Electronics-Devices, Circuits and Industrial Applications*", Oxford University Press, 2010.
3	Ned Mohan, T. M. Undeland, W. P. Robbins, "*Power electronics-Converters, Applications and Design*", Third Edition, John Wiley and Sons Inc., 2003.
4	

	Useful Links
1	https://nptel.ac.in/courses/108/105/108105066/#
2	https://nptel.ac.in/courses/108/108/108108077/
3	https://nptel.ac.in/courses/108/102/108102145/
4	

CO-PO Mapping

	Programme Outcomes (PO)												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	2														
CO2	2	3	1											2	
CO3	2	3													
CO4		2	2											2	

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High
Each CO of the course must map to at least one PO.

Assessment

The assessment is based on MSE, ISE and ESE.
MSE shall be typically on modules 1 to 3.
ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.
ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.
For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

Walchand College of Engineering, Sangli

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AY 2023-24

Course Information	
Programme	B.Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem VII
Course Code	5EN404
Course Name	Real Time Operating System
Desired Requisites:	C programming , Embedded System Design

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	- Hrs/week	30	20	50	100
		Credits: 3			

Course Objectives	
1	To make students familiar with installation and use of the Linux/ Embedded Linux operating system.
2	To give exposure for Embedded Linux boards as per the industry trends
3	To explain /demonstrate services provided by RTOS and their usage
4	To illustrate/demonstrate how to design of applications using RTOS.(uCOS-II)

Course Outcomes (CO) with Bloom's Taxonomy Level		
At the end of the course, the students will be able to,		
CO1	Illustrate various OS, Linux commands ,Embedded Linux Board and concepts of RTOS	Understand
CO2	Write program/ problem/ situation by applying the knowledge acquired in Linux/ RTOS	Apply
CO3	Design the tasks and their interactions by using appropriate RTOS services for multitasking based (RTOS based) embedded system	Create

Module	**Module Contents**	**Hours**
I	Introduction to Operating System: Introduction to OS, Types of OS, Comparison of different OS, Linux Distributions, Linux architecture, Linux Kernel, File Systems, Shell utility, Installation and Configuration of Linux, Basic commands of Linux, Application programming in Linux, multifile programming	7
II	Introduction to Embedded Linux : Embedded Linux introduction, Why Embedded Linux? Linux vs. Embedded Linux, Components of Embedded Linux Systems, , Embedded Linux Boot flow Process, Embedded Linux Boards- Raspberry Pi /Beagle Bone, Raspberry Pi / Beagle Bone - OS installation and configuration, Facilities in Embedded Linux Boards used in Industry/Market	7
III	Introduction to Real-time OS and Real Time system contents RTOS Introduction, Foreground/Background Systems, Pre-emptive and Non-Pre-emptive Kernels, Priority inversion, Deadlock	6
IV	Task Management in RTOS: Task structure, RTOS initialization, Task stack, Task states and task state transitions. Creating and deleting a task, Task priority, Case studies of task-based applications	7

V	Time and Event management in RTOS Clock tick, delaying a task, resuming the delayed task, getting system time, case study of application based on time management	7
VI	Intertask Communication in RTOS Need of Intertask communication, Semaphore, Mailbox, Queues in RTOS. Internals of RTOS for managing tasks and Intertask communication, Case study of RTOS applications.	6

Textbooks	
1	"Mastering Embedded Linux Programming", Second Edition, Chris Simmonds.
2	"MicroC OS II: The Real Time Kernel" Jean J. Labrosse, CMP books publication ISBN: 978-1578201037
3	"Simple Real-time Operating System: A Kernel," Chowdary Venkateswara Amazon, ISBN: 978-1425117825
4	"Real-Time Concepts for Embedded Systems," Qing Li, Caroline Yao Elsevier ISBN: 978-1578201242
References	
1	https://www.engineersgarage.com/embedded-linux-tutorial-basics/
2	"Exploring Raspberry Pi: Interfacing to the Real World with Embedded Linux" first Edition, Derek Molloy
3	https://freertos.org/Documentation/161204_Mastering_the_FreeRTOS_Real_Time_Kernel, A_Hands-On_Tutorial_Guide.pdf
4	www.micrium.com for uCOS-II related documents, tutorials, downloads.
Useful Links	
1	https://www.linux.org/
2	www.nxp.com for processor specific documents.
3	www.NPTEL.org for OS and RTOS related video courses

CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3													
CO2		3												2
CO3			2											2
CO4														

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO.

Assessment

The assessment is based on MSE, ISE and ESE.
MSE shall be typically on modules 1 to 3.
ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.
ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.
For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

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AY 2023-24

Course Information	
Programme	B. Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem.VII
Course Code	5EN403
Course Name	Humanities -4 Legal, IPR, Safety
Desired Requisites:	

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	1 Hrs/Week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	15	10	25	50
Practical	-				
Interaction		**Credits: 1**			

Course Objectives	
1	To introduce the students about Legal, IPR, Safety laws.
2	To disseminate knowledge on patents, patent regime in India and abroad and registration aspects.
3	To be aware about current trends in IPR and Govt. steps in fostering IPR.
4	

Course Outcomes (CO) with Bloom's Taxonomy Level		
At the end of the course, the students will be able to,		
CO1	Understand about Indian industry Legal, IPR, Safety laws	Understand
CO2	Interpret patent and copyright in innovative research work.	Apply
CO3	Illustrate the importance of Indian industry Legal, IPR, Safety laws	Analyze
CO4		

Module	**Module Contents**	**Hours**
I	Overview of Bureau of Indian Standards Act of 1986	2
II	The Right to Information Act of 2005, In order to promote public education andpublic safety	2
III	Intellectual Property, Patents, Copyrights, Trademarks,	3
IV	Other forms of IP, Current Contour,	3
V	The Factories Act, 1948, The Mines Act, 1952,	2
VI	The Dock Workers (Safety, Health & Welfare) Act, 1986.	1

Text Books	
1	Nithyananda, K V. (2019). Intellectual Property Rights: Protection and Management. India, IN: Cengage Learning India Private Limited.
2	D.S. S. Ganguly and C S Changeriya Labor & Industrial Acts & Laws (Safety Management)
3	
4	

5	
References	
1	Ahuja, V K. (2017). Law relating to Intellectual Property Rights. India, IN: Lexis Nexis
2	
3	
4	
Useful Links	
1	Cell for IPR Promotion and Management (http://cipam.gov.in/)
2	https://law.resource.org/pub/in/bis/manifest.med.html
3	World Intellectual Property Organization (https://www.wipo.int/about-ip/en/)
4	Office of the Controller General of Patents, Designs & Trademarks (http://www.ipindia.nic.in/)
5	https://labour.gov.in/industrial-safety-health

CO-PO Mapping														
	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1								1					1	1
CO2									2					2
CO3							1						2	
The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High Each CO of the course must map to at least one PO.														

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AY 2023-24

Course Information

Programme	B. Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem. VII
Course Code	5EN451
Course Name	Power Electronics and Drives Lab
Desired Requisites:	Basic Electrical Engineering, Circuit Theory

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	-	**LA1**	**LA2**	**ESE**	**Total**
Tutorial	-	30	30	40	100
Practical	2 Hrs/Week				
Interaction	-	**Credits: 1**			

Course Objectives

1	**Explain** the V-I characteristics of power semiconductor devices and their use as a switch.
2	**Demonstrate** the operating and handling procedure (i.e. safety measures) of power electronic experimental set ups.
3	**Explain** the need of isolating power circuit ground and control circuit ground (use of Powerscope or isolation transformer) during observation of waveforms and measurement of input and output voltage of a power electronic circuit i.e. controlled rectifier, inverter and chopper.
4	**Demonstrate** the use of simulation software (PSIM, MATLAB, PSPICE) in the analysis and design of power electronic circuits /systems.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**Experiment with** power semiconductor devices and plot its V-I characteristics.	Understand
CO2	**Build** and **test** power electronic circuits (controlled rectifiers, inverters, choppers)	Apply
CO3	**Analyze** the performance power electronic circuits (controlled rectifiers, inverters, choppers)	Analyze
CO4	**Examine** and **compare** speed control techniques/ methods for AC and DC motors.	Analyze

List of Experiments / Lab Activities

The primary objective of this laboratory is to impart the practical knowledge of power electronic circuits for the conversion and control of electrical energy. This laboratory course develops a basic foundation for analysis, design, test, and control of power electronics converters by experimentation and simulation.

List of Experiments: (Minimum 8 experiments)

1. Study of power semiconductor devices: SCR, Power MOSFET, IGBT.
2. SCR triggering circuits: R, RC, and UJT
3. Single phase half controlled bridge rectifier.
4. Single phase fully controlled bridge rectifier.
5. Single phase transistorized inverter.
6. Single phase to Single phase Cycloconverter.
7. Design and implementation of a Type-A chopper (Power MOSFET based) circuit.
8. Single/ Three phase controlled rectifier fed DC drive.
9. Chopper fed DC drive.
10. Three phase induction motor drive.
11. Four quadrant DC drive (Dual converter).
12. Speed control of brushless DC motor.
13. Simulation of Controlled Rectifier and Three Phase Inverter Circuit using MATLAB/ PSIM.

Text Books

1	M.H. Rashid, "*Power Electronics: Circuits, Devices & Applications*", Third Edition, PHI, New Delhi, 2008.

2	M. D. Singh & K. B. Khanchandani, "*Power Electronics*", Second Edition, Tata McGraw-Hill Publishing Company Ltd., New Delhi, 2007.
3	V. R. Moorthi, "*Power Electronics: Devices, Circuits and Industrial Applications*", Oxford University Press, 2010.
4	

References	
1	D. R. Grafham, J. C. Hey, "*SCR Manual*", Fifth Edition, General Electric, New York, 1972.
2	https://www.powersimtech.com/wp-content/uploads/2021/01/PSIM-User-Manual.pdf
3	
4	

Useful Links	
1	https://powersimtech.com/products/psim/capabilities-applications/
2	https://in.mathworks.com/solutions/power-electronics-control/power-electronics-simulation.html
3	https://www.plexim.com/products/plecs
4	

CO-PO Mapping

	Programme Outcomes (PO)												**PSO**		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	1			3											
CO2				3	3									2	
CO3		1		3	3									2	
CO4	1			3	2										

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High
Each CO of the course must map to at least one PO.

Assessment

There are three components of lab assessment, LA1, LA2 and Lab ESE.
IMP: Lab ESE is a separate head of passing. LA1, LA2 together is treated as In-Semester Evaluation.

Assessment	**Based on**	**Conducted by**	**Typical Schedule**	**Marks**
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 6 Marks Submission at the end of Week 6	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 7 to Week 12 Marks Submission at the end of Week 12	30
Lab ESE	Lab activities, attendance, journal	Lab Course Faculty	During Week 15 to Week 18 Marks Submission at the end of Week 18	40

Week 1 indicates starting week of a semester. The typical schedule of lab assessments is shown, considering a 26-week semester. The actual schedule shall be as per academic calendar. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments.

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AY 2023-24

Course Information

Programme	B.Tech. (Electronics Engineering)
Class, Semester	FinalYear B. Tech., Sem VII
Course Code	5EN452
Course Name	Real Time Operating System Lab
Desired Requisites:	Theory/Lab Courses with C programming, Microcontroller Peripherals and Interfacing, Embedded System Design.

Teaching Scheme		**Examination Scheme (Marks)**			
Practical	2 Hrs/ Week	**LA1**	**LA2**	**Lab ESE**	**Total**
Interaction	- Hrs/ Week	30	30	40	100
		Credits: 1			

Course Objectives

1	To learn system Architecture, configuration and Programming for Embedded Linux Based System.
2	To facilitate students to gain practical experience of RTOS and services provided by it.
3	To help students to co-relate the RTOS theory with the RTOS implementation.
4	To provide exposure to industry applications and facilitate for writing applications using Linux and RTOS.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Installation of OS Process and write programs / scripts for Embedded Linux Board.	Apply
CO2	Verify the RTOS fundamentals, through illustrative programs and demonstrate usage of task, time, and event management, Intertask communication using a simulator. (Programming skill, Modern Tools)	Analyze
CO3	Implement a given logic as an RTOS based application. Create document of the same and demonstrate using simulation tools. (Programming skill, Independent and teamwork, Modern Tools)	Create

List of Experiments / Lab Activities/Topics

List of Topics(Applicable for Interaction mode):

List of Lab Activities:

1. Experiments to revise an Embedded System Design
2. Experiment to study Linux distribution installation, configuration and basic commands of it.
3. Experiment to study configuration for an Embedded Linux Board.
4. Experiment to access GPIO of an Embedded Linux Board to control components / devices interfaced to it.
5. Demonstration of RTOS based application in keil micro vision
6. Writing of RTOS based application .
7. Finding the type of kernel for a given RTOS (Pre-emptive or Non-pre-emptive)
8. Semaphore for managing shared resource and task synchronization
9. Demonstration of Clock tick and its effect of event timing in RTOS based systems.
10. Semaphore for event synchronization
11. Using mailbox facility in RTOS
12. Using queue facility in RTOS
13. Avoiding deadlock in RTOS

Textbooks

1	"Mastering Embedded Linux Programming", Second Edition, Chris Simmonds.

2	"Exploring Raspberry Pi: Interfacing to the Real World with Embedded Linux" first Edition, Derek Molloy
3	*"MicroC OS II: The Real Time Kernel"* Jean J. Labrosse, CMP books publication ISBN: 978-1578201037
4	*RTOS Lab Manual*
References	
1	https://www.engineersgarage.com/embedded-linux-tutorial-basics/
2	www.micrium.com for uCOS-II related documents, tutorials, downloads.
3	https://www.freertos.org/Documentation/RTOS_book.html
4	Everything You Need to Know about RTOS (pdf book) by Silabs
Useful Links	
1	https://www.linux.org/
2	https://www.raspberrypi.org/
3	www.highintegritysystems.com/rtos for RTOS tutorials
4	https://www.youtube.com/watch?v=ECEvUEkSSLg for videos by Renesas Inc.

CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1		3												
CO2			3										2	
CO3				2					2					2

The strength of mapping is to be written as 1,2,3; where, 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO, and preferably to only one PO.

Assessment

There are three components of lab assessment, LA1, LA2 and Lab ESE.
IMP: Lab ESE is a separate head of passing.(min 40 %), LA1+LA2 should be min 40%

Assessment	Based on	Conducted by	Typical Schedule	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 8 Marks Submission at the end of Week 8	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 9 to Week 16 Marks Submission at the end of Week 16	30
Lab ESE	Lab activities, journal/ performance	Lab Course Faculty and External Examiner as applicable	During Week 18 to Week 19 Marks Submission at the end of Week 19	40

Week 1 indicates starting week of a semester. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming, and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments and related activities if any.

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AY 2023-24

Course Information

Programme	B. Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech. Sem. VII
Course Code	5EN446
Course Name	Project-I
Desired Requisites:	Mini-Project

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	-	**LA1**	**LA2**	**ESE**	**Total**
Tutorial	-	30	30	40	100
Practical	6 Hrs/Week				
Interaction	-	**Credits: 3**			

Course Objectives

1	**Explain** to survey and study the published literature on the assigned/ selected topic. The topic may be chosen from the problem assigned by the industry. The chosen topic may provide a solution to the electronics industry problem/ solution to societal needs.
2	**Explain** the use of methods/ methodology/ procedures/ software tools to carry out preliminary **Analysis**/ **Modelling**/ **Simulation**/ Experiment/ Design. It is expected to find out the feasibility of the project.
3	**Illustrate** the guidelines to write and **organize** the project report based on the study conducted for presentation to the department.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**Explain** the purpose of the project and conceptual idea behind the project.	Understand
CO2	**Analyze** the journal/ conference/ research papers/ magazine articles and present the comparative study of similar work done by others.	Analyze
CO3	**Propose** a research problem/ problem undertaken as project-work and present it in a clear and distinct manner through different **design techniques** which meets the desired objectives of the project-work.	Create
CO4	Prepare **and Organize** written report on the study conducted/part of project-work (simulations/ technical design) completed for presentation before the department committee.	Apply

List of Experiments / Lab Activities

The objective of Project-I is to enable the student to take up investigative study in the broad field of Electronics Engineering, either fully theoretical/practical or involving both theoretical and practical work to be assigned by the Department on an individual basis or three/five students in a group, under the guidance of a Supervisor from the Department alone or jointly with a Supervisor/ Mentor from Industry. This is expected to provide a good initiation for the student(s) in R&D work.

The Projects may be chosen from the following areas/domains, but not limited to:

- Embedded Systems/ VLSI Design
- Electronic Communication Systems
- Biomedical Electronics
- Power Electronics/ Electric Vehicles
- Robotics and Mechatronic Systems
- Artificial Intelligence and Machine Learning
- Applications of Electronics to Agriculture

Assessment: A demonstration and oral examination on the Project-I shall be conducted at the end of the semester.

Text Books

1	Journal/ Conference papers/ Magazine Articles/ Handbooks with reference to topic selected for the project-work.
2	
3	
4	
References	
1	Journal/ Conference papers/ Magazine Articles/ Handbooks with reference to topic selected for the project-work.
2	
3	
4	
Useful Links	
1	https://ieeexplore.ieee.org
2	https://www.sciencedirect.com
3	https://www.elsevier.com
4	

CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3					3	2			2			2	2
CO2		3		3									3	3
CO3			3		2								3	3
CO4								2	3	3	3	2	2	2

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High
Each CO of the course must map to at least one PO.

Assessment

There are three components of lab assessment, LA1, LA2 and Lab ESE.
IMP: Lab ESE is a separate head of passing. LA1, LA2 together is treated as In-Semester Evaluation.

Assessment	Based on	Conducted by	Typical Schedule	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 6 Marks Submission at the end of Week 6	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 7 to Week 12 Marks Submission at the end of Week 12	30
Lab ESE	Lab activities, attendance, journal	Lab Course Faculty	During Week 15 to Week 18 Marks Submission at the end of Week 18	40

Week 1 indicates starting week of a semester. The typical schedule of lab assessments is shown, considering a 26-week semester. The actual schedule shall be as per academic calendar. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments.

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AY 2023-24

Course Information

Programme	B. Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem.VII
Course Code	5EN455
Course Name	Humanities -3 Project Management
Desired Requisites:	

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture		**LA1**	**LA2**	**ESE**	**Total**
Tutorial	-	15	15	20	50
Practical	-				
Interaction	1 Hrs/Week	**Credits: 1**			

Course Objectives

1	To prepare the students to manage projects by exploring both technical and managerial challenges and preparing the budget.
2	To make aware the students about leadership and ethical qualities in dealing with real life project
3	To induce qualities for working in interdisciplinary and cross functional teams with effective Communication skills, economical and managerial challenges and commercial management.
4	

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Grasp and perceive the project activities with respect to resources required and the constraint for feasibility or completion within time	Understand
CO2	Estimate and prepare budget for project completion, Understand commercial management	Analyze
CO3	Figure out and schedule the project and assess for controlling critical path networks	Evaluate
CO4		

Module	**Module Contents**	**Hours**
I	Introduction to Project Management.	2
II	Project Cost, Planning, feasibility, risk.	2
III	Critical Path Networks - Principles of Resource Scheduling.	2
IV	Executing and Controlling.	2
V	Commercial Management and various regulations.	2
VI	Study and use of software related to Project Management System.	3

Text Books

1	Dennis Lock , Project Management - Gower Publishing Limited, 2013
2	Samuel J. Mantel, Jr., Jack R. Meredith, Scott M. Shafer, Margaret M. Sutton , Project Management in Practice - JOHN WILEY & SONS, INC., 2011
3	B.C. Punmia and Khandelwal, Project Planning and Control with PERT and CPM, Lakshmi Publications Pvt. Ltd., 2001
4	HoraldKerzner, Project Management: A systems approach to planning, scheduling and controlling, John Wiley & Sons Inc., 2009
5	The factories act 1948 – Government of India 6. Meri Williams , The Principles of Project Management By – SitepointPvt Ltd., 2008

References

1	K. Nagarajan, Project Management, New Age Int., 2nd ed. 2004.
2	B.M.Naik, Project Management-Scheduling and Monitoring by PERT/CPM, 1984
3	William R Duncan, A guide to the project management body of knowledge, PMI Publications, 1996
4	

Useful Links	
1	https://www.apm.org.uk/resources/what-is-project-management/
2	https://www.projectmanager.com/project-management
3	
4	

CO-PO Mapping

	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1								1					1	1
CO2									2					2
CO3							1						2	

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High
Each CO of the course must map to at least one PO.

Walchand College of Engineering, Sangli

(Government Aided Autonomous Institute)

AY 2023-24

Course Information	
Programme	B.Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem VII
Course Code	5EN414
Course Name	Professional Elective 5-Microwave Engineering
Desired Requisites:	Communication Engineering

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-Hrs/week	30	20	50	100
		Credits: 3			

Course Objectives	
1	To understand the theoretical principles underlying microwave devices and networks
2	To introduce the various types of transmission lines and to discuss the losses associate
3	To instill knowledge on the properties of various microwave components
4	To deal with the microwave generation and microwave measurement techniques

Course Outcomes (CO) with Bloom's Taxonomy Level		
At the end of the course, the students will be able to,		
CO1	Classify the microwave frequencies and the waveguides that are used application	Understand
CO2	Examine the active & passive microwave devices & components used in Microwave communication systems	Analyze
CO3	Analyze the operation and working of the various tubes or sources for the transmission of the microwave frequencies	Analyze
CO4	Measure the various microwave parameter using analytical treatment	Evaluate

Module	**Module Contents**	**Hours**
I	**Microwave Fundamentals and Electromagnetic field Theory** Microwave regions and band designations, microwave devices, applications of microwaves, Interaction between electrons and fields, electron motion in electric, magnetic and electromagnetic field, electromagnetic plane waves	5
II	**Microwave Waveguide and Components** Rectangular and circular waveguide, TE and TM modes, power transmission and power losses in waveguide, excitation modes in waveguide, microwave cavities, Microwave passive components—Tee junctions, magic tee, couplers, circulators, attenuators, phase shifters, bends, twists, corners, irises, windows. Scattering Matrix Parameters of microwave networks, S-matrix for E-plane Tee junction, S-matrix for H-plane Tee junctions, S-matrix for directional coupler	8
III	**Microwave Tubes** Limitations of conventional tubes, O and M type classification of microwave tubes, re-entrant cavity, velocity modulation. Types of Tubes, Two cavity Klystron, Reflex Klystron, traveling wave tube amplifier, Magnetron	6
IV	**Microwave Solid State Devices** Tunnel diode, PIN diode, Gunn diode, LSA diode, Read diode, IMPATT diode, TRAPATT diode, BARITT DIODE, Varactor Diode, solid state ruby laser, semiconductor laser	7

V	**Microwave Measurements** Measurement devices: Slotted line, Tunable detector, VSWR meter, Power Meter, S-parameter measurement, frequency measurements, Power measurement, Attenuation measurement, Phase shift measurement, VSWR measurement, Impedance measurement, Q of cavity resonator measurement	7
VI	**Microwave Strip Lines and Antenna** Micro-strip line, Slot line, Parallel strip line, advantages, Horn antenna, Dish Antenna, Micro-strip antenna	6

Textbooks	
1	Microwave Engineering, 4th Edition, Pozar, D.M., 2011, Wiley (ISBSN - 9781118213636)
2	FOUNDATIONS FOR MICROWAVE ENGINEERING, 2ND ED, By Robert E. Collin, John Wiley & Sons, 2007, (ISBN: 8126515287)
3	RF and Microwave Engineering: Fundamentals of Wireless Communications, Gustrau, F, 2012, Wiley, ISBN - 9781118349571
4	

References	
1	Microwave and Radar Engineering, By Gottapu Sasibhushana Rao · 2014, Pearson Education India, (ISBN: 9789332540637)
2	Microwave Engineering, Das, A., and Das, S.K., McGraw-Hill, 2000, (ISBN - 9780074635773)
3	Microwave Engineering, S Vasuki and D Helena Margaret, R Rajeswari, McGraw Hill Education (India) Private Limited, ISBN933921949X, 9789339219499
4	

Useful Links	
1	https://onlinecourses.nptel.ac.in/noc20_ee91/preview
2	
3	
4	

CO-PO Mapping

	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3													
CO2				3										
CO3				3										
CO4				3										

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO.

Assessment

The assessment is based on MSE, ISE and ESE.
MSE shall be typically on modules 1 to 3.
ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.
ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.
For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

Walchand College of Engineering, Sangli

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AY 2023-24

Course Information	
Programme	B.Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem VII
Course Code	5EN415
Course Name	Professional Elective 5- TCP IP and Advanced Protocol
Desired Requisites:	Digital Communication

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	_Hrs/week	30	20	50	100
		Credits: 3			

Course Objectives	
1	To develop an understanding of computer networking basics
2	To be exposed to the TCP/IP protocol suite
3	To develop an understanding of different components of computer networks, various protocols, modern technologies and their applications.
4	To gain conceptual understanding of Software Defined Networks (SDN)

Course Outcomes (CO) with Bloom's Taxonomy Level		
At the end of the course, the students will be able to,		
CO1	Design a small TCP/IP Network	Apply
CO2	Identify security issues and suggest suitable solution	Analyze
CO3	Explain concept of cloud and its models.	Understand
CO4	Explain OpenFlow challenges in SDN, and developments in SDN	Understand

Module	**Module Contents**	**Hours**
I	**Introduction to Network and Data Link Layer** Introduction to Network, Transmission media, Topology, Switching techniques. OSI Model, TCP/IP Model Data Link layer design issues, Logical Link Control, Medium Access Control, Elementary Data link layer protocols, Sliding window protocol , Medium access sub layer- Multiple access protocols.	7
II	**Internet Protocol : IPv4 :** IP Datagram Formats - Data and Fragmentation - Address Masks- Prefixes- and Subnetworks - Network Address Translation (NAT) - IP Switching and Routing - Local Delivery and Loopbacks - Address Resolution Protocol ICMP.	8
III	**Transport Layer protocols** UDP and TCP segments, comparison, TCP state flow diagram, TCP flow control, congestion control, error control. TCP Timers.	7
IV	**Application Layer protocols:** Audio video streaming over IP (RTP,RTCP, SCTP), Application layer protocols, HTTP, SMTP, SNMP, FTP.	6
V	**Security:** The Need of Security, Security Approaches, Principal of Security, Types of Attacks. Network Security: Brief Introduction to Firewalls, IP Security, Virtual Private Networks (VPN)	6

VI	**Cloud Computing and Software Defined Networking(SDN)**: Business Drivers - Technology Innovations - Basic Concepts and Terminology Cloud Characteristics - Cloud Delivery Models - Cloud Deployment Models. Basics and Open flow, SDN Controller, SDN challenges, SDN and virtualization.	6

Textbooks	
1	” Computer Networks”, B A Forouzan McGraw Hill Education 2016
2	Software defined Networking, Chuck Black Elsevier 2014
3	
4	
References	
1	Wayne Tomasi, “Introduction to Data Communication and Networking”, 1/e, Pearson Education .
2	Greg Tomsho, Ed Tittel, David Johnson. “Guide to Networking Essentials”, fifth edition, Thomson India Learning, 2007.
3	
4	
Useful Links	
1	https://www.cloudflare.com/en-in/learning/ddos/glossary/tcp-ip/
2	https://networkengineering.stackexchange.com/questions/63278/what-layers-of-the-tcp-ip-model- does-an-sdn-involve
3	
4	

CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1			2										2	
CO2		2												1
CO3		1												1
CO4	1	1												1

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO.

Assessment

The assessment is based on MSE, ISE and ESE.
MSE shall be typically on modules 1 to 3.
ISE shall be taken throughout the semester in the form of teacher’s assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.
ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.
For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

Walchand College of Engineering, Sangli

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AY 2023-24

Course Information

Programme	B. Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem. VII
Course Code	5EN416
Course Name	Professional Elective 5-Analog CMOS IC Design
Desired Requisites:	Digital Electronics, Digital CMOS IC Design

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
Practical	-				
Interaction	-	**Credits: 3**			

Course Objectives

1	To **explain** the analog circuit concepts based on MOS devices in such a way to develop in students the insight and intuition towards MOS circuits.
2	To **organize** guest lectures and practical sessions with the help of industry persons.
3	To **deliver** the tips (or thumb rules) related with design of analog circuits throughout the course.
4	To **motivate** the students to develop lifelong/ self-learning attitude.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**Analyze** MOS device circuits to derive the dependence of various electrical parameters analytically and graphically. (M1)	Analyze
CO2	**Develop** large signal and small signal models for single stage amplifiers and differential amplifiers using MOS transistors and derive the gain relationships. (M2, M3)	Apply
CO3	**Design** common source, common gate, common drain amplifier for given specifications. Further recognize their application under various typical situations. (M2, M3)	Design
CO4	**Analyze** large signal and small signal behaviour of differential amplifiers and compute the differential gain, common mode gain and CMRR. (M3)	Analyze
CO5	**Analyze** active current mirrors and explain the properties of differential pairs using such circuits as loads. (M5)	Analyze
CO6	**Design** 2-stage Op-Amp for given specifications. **Compute** the poles and zeros in the frequency response of the single stage amplifiers using time-constant method (M6)	Design

Module	**Module Contents**	**Hours**
I	**MOS Device Physics** MOS IV Characteristics, Second Order Effects, MOS device models (MOS device capacitance, MOS small signal model) MOS model parameters	8
II	**Single Stage Amplifier** Part I CS stage with resistance load, diode connected load, current source load, , CS stage with source, degeneration,	6
III	**Single Stage Amplifier** Part II source follower, common-gate stage, Cascode stage, folded cascade, choice of device models.	6
IV	**Differential Amplifiers** Basic difference pair, differential mode response, common mode response, Differential pair with MOS loads	6
V	**Passive and Active Current mirrors** Basic current mirrors, Cascode mirrors, active current mirrors.	7
VI	**Frequency Response** CS stage, Source follower, Common gate stage, Cascode stage and Difference pair. Design of 2-stage operational amplifier	7

Text Books	
1	Behzad Razavi, "*Design of Analog CMOS Integrated Circuits"*, Second Edition, Tata McGraw-Hill Publishing Company Limited, New Delhi, 2017.
2	
3	
4	
References	
1	R. Jacob Baker, "*CMOS: Circuit Design, Layout and Simulation*", Wiley-Inter- science, (2008)
2	Allen, P.E. and Holberg, D.R., "*CMOS Analog Circuit Design*", Oxford University Press (2002)
3	
4	
Useful Links	
1	www.vlsi-expert.com,
2	www.testbench.in
3	www.asic-world.com
4	https://nptel.ac.in/courses/117/101/117101105/

CO-PO Mapping

	Programme Outcomes (PO)												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	2	3												3	
CO2	2	3												3	
CO3			3											3	
CO4	2	3												3	
CO5	2	3												3	
CO6		2	3											3	

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High
Each CO of the course must map to at least one PO.

Assessment

The assessment is based on MSE, ISE and ESE.
MSE shall be typically on modules 1 to 3.
ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.
ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.
For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

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AY 2023-24

Course Information	
Programme	B.Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem VII
Course Code	5EN454
Course Name	Professional Elective 5 -Microwave Engineering Lab
Desired Requisites:	Communication Engineering

Teaching Scheme		**Examination Scheme (Marks)**			
Practical	2 Hrs/ Week	**LA1**	**LA2**	**Lab ESE**	**Total**
Interaction	- Hrs/ Week	30	30	40	100
		Credits: 1			

Course Objectives	
1	To understand the theoretical principles underlying microwave devices and networks
2	To introduce the various types of transmission lines and to discuss the losses associate
3	To instill knowledge on the properties of various microwave components
4	To deal with the microwave generation and microwave measurement techniques

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Classify the microwave frequencies and the waveguides that are used application	Understand
CO2	Examine the active & passive microwave devices & components used in Microwave communication systems	Analyze
CO3	Analyze the operation and working of the various tubes or sources for the transmission of the microwave frequencies	Analyze
CO4	Measure the various microwave parameter using analytical treatment	Evaluate

List of Experiments / Lab Activities/Topics

List of Topics(Applicable for Interaction mode):

List of Lab Activities:
List of Experiments:

1. Study of Microwave components and equipment

2. Study of V-I Characteristics of Gunn Diode

3. Reflex Klystron as source and plot its various modes

4. Verification of port characteristics of E-plane tee, H-plane tee & Magictree

5. Verification of port characteristics of Microwave Circulator and isolator, calculation of insertion loss and isolation loss

6. Verification of port characteristics of Directional coupler, calculation of coupling factor, insertion loss and directivity.

7. Power pattern of Horn Antenna

8. Power Patterns of different Antenna like Dipole, Yagi etc.

9. Study of slotted section with probe carriage. Measure the VSWR for various values of terminating impedances (open/short/matched termination).

10. To test and verify Microwave Integrated Circuits using Microstrip trainer kit and finds parameters, and plot the frequency response.

Textbooks	
1	Microwave Engineering, 4th Edition, Pozar, D.M., 2011, Wiley (ISBSN - 9781118213636)
2	FOUNDATIONS FOR MICROWAVE ENGINEERING, 2ND ED, By Robert E. Collin, John Wiley & Sons, 2007, (ISBN: 8126515287)
3	RF and Microwave Engineering: Fundamentals of Wireless Communications, Gustrau, F, 2012, Wiley, ISBN - 9781118349571
4	
References	
1	Microwave and Radar Engineering, By Gottapu Sasibhushana Rao · 2014, Pearson Education India, (ISBN: 9789332540637)
2	Microwave Engineering, Das, A., and Das, S.K., McGraw-Hill, 2000, (ISBN - 9780074635773)
3	Microwave Engineering, S Vasuki and D Helena Margaret, R Rajeswari, McGraw Hill Education (India) Private Limited, ISBN933921949X, 9789339219499
4	
Useful Links	
1	https://onlinecourses.nptel.ac.in/noc20_ee91/preview
2	
3	
4	

CO-PO Mapping														
	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3													
CO2				3										
CO3				3										
CO4				3										
The strength of mapping is to be written as 1,2,3; where, 1: Low, 2: Medium, 3: High Each CO of the course must map to at least one PO, and preferably to only one PO.														

Assessment				
There are three components of lab assessment, LA1, LA2 and Lab ESE. IMP: Lab ESE is a separate head of passing.(min 40 %), LA1+LA2 should be min 40%				
Assessment	**Based on**	**Conducted by**	**Typical Schedule**	**Marks**
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 8 Marks Submission at the end of Week 8	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 9 to Week 16 Marks Submission at the end of Week 16	30
Lab ESE	Lab activities, journal/ performance	Lab Course Faculty and External Examiner as applicable	During Week 18 to Week 19 Marks Submission at the end of Week 19	40
Week 1 indicates starting week of a semester. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming, and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments and related activities if any.				

Walchand College of Engineering, Sangli

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AY 2023-24

Course Information	
Programme	B.Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem VII
Course Code	5EN458
Course Name	Professional Elective 5 Lab TCP IP and Advanced Protocol Lab
Desired Requisites:	Digital Communication, Data Communication

Teaching Scheme		**Examination Scheme (Marks)**			
Practical	2 Hrs/ Week	**LA1**	**LA2**	**Lab ESE**	**Total**
Interaction	- Hrs/ Week	30	30	40	100
		Credits: 1			

Course Objectives	
1	To provide understanding of the protocol concepts.
2	To demonstrate PC-PC communication.
3	To understand applications of TCP-IP networking.
4	

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Design basic protocol	Apply
CO2	Compare various communication protocols	Analyze
CO3	Simulate/Design applications for TCP-IP protocol suite.	Create
CO4		

List of Experiments / Lab Activities/Topics

List of Topics(Applicable for Interaction mode):

List of Lab Activities:

Perform/ simulate 8 to 10 experiments on following points

List of Experiments:

1. Simulate / Implement Data Link Layer protocols
   a. Stop and Wait
   b. GO Back N
   c. Selective Repeat
2. IP datagram Analysis using Wireshark/ TCP dump.
   a Non Fragmented datagram/ Fragmented datagram
   b. TTL, Address, FLAG field analysis
3. TCP handshaking process connection establishment process
4. Socket Programming UDP/TCP
5. Campus wide network study with VLANs
6. Study Firewall configuration and implementation
7. Study of Open Flow concept
8. Study of cloud architecture and services

Textbooks

1	1 "Data Communication and Networking" ,TMH, B. Forouzan
2	2 "TCP/IP Protocol Suite", TMH, B. Forouzan
3	
4	

References

1	“Internetworking with TCP/IP”, Pearson, Douglas Comer
2	William Stallings “Foundations of Modern Networking : SDN, NFV, QoE, IoT and Cloud” Pearson Education
3	
4	
Useful Links	
1	
2	
3	
4	

CO-PO Mapping														
	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1			3											2
CO2				3										
CO3									3				2	
CO4														
The strength of mapping is to be written as 1,2,3; where, 1: Low, 2: Medium, 3: High Each CO of the course must map to at least one PO, and preferably to only one PO.														

Assessment				
There are three components of lab assessment, LA1, LA2 and Lab ESE. IMP: Lab ESE is a separate head of passing.(min 40 %), LA1+LA2 should be min 40%				
Assessment	**Based on**	**Conducted by**	**Typical Schedule**	**Marks**
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 8 Marks Submission at the end of Week 8	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 9 to Week 16 Marks Submission at the end of Week 16	30
Lab ESE	Lab activities, journal/ performance	Lab Course Faculty and External Examiner as applicable	During Week 18 to Week 19 Marks Submission at the end of Week 19	40
Week 1 indicates starting week of a semester. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming, and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments and related activities if any.				

Walchand College of Engineering, Sangli

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AY 2023-24

Course Information

Programme	B. Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem. VII
Course Code	5EN457
Course Name	Professional Elective 5 Lab -Analog CMOS IC Design Lab
Desired Requisites:	Digital Electronics, Digital CMOS IC Design

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	-	**LA1**	**LA2**	**ESE**	**Total**
Tutorial	-	30	30	40	100
Practical	2 Hrs/Week				
Interaction	-	**Credits: 1**			

Course Objectives

1	**Demonstrate** the flow of Cadence EDA tools for designing and simulating analog CMOS circuits.
2	**Develop** an insight into CMOS analog circuits and design single stage CS, CG, CD, differential amplifiers and 2-stsge Operational amplifier for given specifications.
3	**Explain** how to characterize the transistors for the voltage conditions seen by the circuit with goal of optimizing dimensions for given ID or trans-conductance.
4	**Prepare** the students for good documentation discipline.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**Analyze** MOS transistors for targeted value of g_m or drain current for designing the physical dimensions and the required gate bias using Cadence EDA tools.	Analyze
CO2	**Demonstrate** the complete flow of Cadence tools from schematic to symbol generation to simulation for CS, CG, CD and differential amplifiers	Understand
CO3	**Build** and **simulate** the single stage amplifier circuits (CS, Source Follower, Cascode stage, differential pair etc.) using MOSFETs schematic design entry for various loads and relate the gain values with theoretical expressions.	Apply
CO4	**Design** differential pair circuits with active current mirror load for given gain and UGB.	Create
CO5	**Design**, **build** and **simulate** 2-stage operational amplifier for given pole frequencies and UGB with and without pole splitting and pole-zero compensation.	Create

List of Experiments / Lab Activities

List of Experiments:

1. Characterize nMOS transistors from schematic using Cadence tools.
2. Design, build and simulate single stage Common Source amplifier using resistive load and nMOS diode connected load (Gain and Frequency response). Compare the performance with pMOS diode connected load.
3. Design, build and simulate Common Source amplifiers with current source load. Compare the performance with already studied loads.
4. Design, build and simulate Common Source stage with source degeneration. (gain and frequency response) Compare the performance with and without source degeneration.
5. Design, build and simulate Source follower /Common Gate stage. Crosscheck the results of output impedance, gain, power dissipation against theoretical expectations.
6. Design, build and simulate cascode stage with different loads for the specified voltage gain and maximum power dissipation.
7. Design, build and simulate differential pair with specified tail current source and maximum full swing differential gain using, a)resistive load and b) pMOS current source load and compare the gain values. Cross-confirm the results against theoretical expectations.

8. Demonstrate the design of differential pair with active tail current source (replace the tail current source in Expt. 8 by a nMOS current source biased in saturation). Simulate for evaluating differential gain, common mode gain and CMRR.
9. Design, build and simulate differential amplifier (single ended output) with active current mirror load for the given specifications. Evaluate for CMRR, DC gain etc.
10. Demonstrate design of 2-stage operational amplifier for given UGB.

Text Books	
1	Behzad Razavi, "*Design of Analog CMOS Integrated Circuits"*, Second Edition, Tata McGraw-Hill Publishing Company Limited, New Delhi, 2017.
2	
3	
4	
References	
1	R. Jacob Baker, "*CMOS: Circuit Design, Layout and Simulation*", Wiley-Inter- science, 2008.
2	Allen, P.E. and Holberg, D.R., "*CMOS Analog Circuit Design*", Second Edition, Oxford University Press, 2002.
3	
4	
Useful Links	
1	www.vlsi-expert.com
2	www.testbench.in
3	www.asic-world.com
4	https://nptel.ac.in/courses/117/101/117101105/

CO-PO Mapping

	Programme Outcomes (PO)												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	1			2	3									3	
CO2				2	3									3	
CO3			2	2	3									3	
CO4				3	3									3	
CO5				3	3									3	

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High
Each CO of the course must map to at least one PO.

Assessment

There are three components of lab assessment, LA1, LA2 and Lab ESE.
IMP: Lab ESE is a separate head of passing. LA1, LA2 together is treated as In-Semester Evaluation.

Assessment	Based on	Conducted by	Typical Schedule	Marks
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 6 Marks Submission at the end of Week 6	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 7 to Week 12 Marks Submission at the end of Week 12	30
Lab ESE	Lab activities, attendance, journal	Lab Course Faculty	During Week 15 to Week 18 Marks Submission at the end of Week 18	40

Week 1 indicates starting week of a semester. The typical schedule of lab assessments is shown, considering a 26-week semester. The actual schedule shall be as per academic calendar. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments.

Walchand College of Engineering, Sangli

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AY 2023-24

Course Information	
Programme	B. Tech.
Class, Semester	Final Year B. Tech., Semester VII
Course Code	5OE457
Course Name	Open Elective 5 – Medical Image Processing
Desired Requisites:	-

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	60	100
Practical	-				
Interaction	-	**Credits: 3**			

Course Objectives	
1	To learn facts about medical imaging sources and study various formats.
2	To study various segmentation and filtering technique of medical image.
3	To learn spatial transformation of medical image

Course Outcomes (CO) with Bloom's Taxonomy Level	
At the end of the course, the students will be able to,	
CO1	Demonstrate various image sources, there representation and various formats of image.
CO2	Apply segmentation, filtering and transformation on medical image.
CO3	Analyse various facts of image registration and CT reconstructed image.
CO4	

Module	**Module Contents**	
I	**Basics of Medical Image Sources:** Radiology, the electromagnetic spectrum, basic x-ray physics, attenuation and imaging, computed tomography, magnetic resonance tomography, ultrasound, nuclear medicine and molecular imaging, other imaging techniques, radiation protection and dosimetry	6
II	**Image Representation:** Pixels and voxels, gray scale and color representation, image file formats, DICOM, other formats, image quality, and the signal-to-noise ratio, the intensity transform function and the, dynamic range, windowing, histograms and histogram operations, dithering and depth	6
III	**Segmentation:** The segmentation problem, roi definition and centroids, thresholding, region growing, more sophisticated segmentation methods, morphological operations	6
IV	**Filtering and Transformations:** The filtering operation, the fourier transform, other transforms, discretization – resolution and artifacts, interpolation and volume regularization, translation and rotation, reformatting, tracking and image-guided therapy	**6**
V	**Rendering and Surface Models:** Visualization, orthogonal and perspective projection, and the viewpoint, ray casting, surface–based rendering **Registration:** Fusing information, registration paradigms, merit functions, optimization strategies, some general comments, camera calibration, registration to physical space	6
VI	**CT Reconstruction:** Introduction, radon transform, algebraic reconstruction, some remarks on fourier transform and Filtering, filtered backprojection	6

Text Books	
1	Wolfgang Birkfellner, Michael Figl, and Johann Hummel, "Applied Medical Image Processing: A Basic Course", CRC Press, Taylor & Francis, 2014.
2	G R Sinha, Bhagwati Charan Patel, "Medical Image Processing", PHI Learning Pvt Ltd. 2014.
3	
References	
1	Geoff Dougherty, "Medical Image Processing", Springer Science and Business Media, 2011
2	Geoff Dougherty, "Digital Image Processing for Medical Applications", Cambridge University Press, 2009.
3	
Useful Links	
1	https://www.coursera.org/
2	
3	
4	

CO-PO Mapping

	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3													
CO2			2											
CO3						2								2
CO4														

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High
Each CO of the course must map to at least one PO.

Assessment

The assessment is based on MSE, ISE and ESE.
MSE shall be typically on modules 1 to 3.
ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.
ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.
For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

Walchand College of Engineering, Sangli

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AY 2023-24

Course Information

Programme	B.Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech. Sem VIII
Course Code	5EN422
Course Name	Internet of Things
Desired Requisites:	Sensors and Instrumentation, Embedded System

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
Practical	-				
Interaction	-	**Credits: 3**			

Course Objectives

1	To provide understanding of the Internet of Things concepts.
2	To demonstrate various IoT communication protocols.
3	To understand applications of Internet of Things and its usefulness for society.
4	

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Explain IoT building blocks	Understand
CO2	Compare various IoT connectivity and communication technologies	Analyze
CO3	Design applications for solution building in IoT domain	Apply

Module	**Module Contents**	**Hours**
I	**IoT Fundamentals and Overview** : Definition and Characteristics of IoT, Physical Design of IoT, IoT enabled Technologies , IoT Applications : Smart cities, Smart Homes, Smart Agriculture, Smart Energy, Smart vehicles	6
II	**IoT Physical Devices and Endpoints**: Mobile Ad hoc Network, Stationary and Mobile Wireless Sensor Networks, Hardware and software architecture of sensor node ,type of sinks, gateway, Operating system for WSN	8
III	**MAC and network layer for sensor network**: IEEE standard Protocols for sensor network communication, low duty cycle protocols and wake up concepts for energy conservation	8
IV	**IoT Communication Technologies**:M2M protocols for IoT- 6LowPAN, RFID, Wireless HART, MQTT, CoAP, XMPP, AMQP	6
V	**Cloud and SDN**: cloud computing and virtualization concepts, Cloud Architecture , Cloud computing, benefits , challenges, risksCloud services , introduction to software defined network	6

VI	**IoT Security and Authentication**: Implementing basic security measures for IoT devices (e.g., encryption, authentication), IoT Data Analytics :basic data analytics on IoT sensor data.	5

Text Books	
1	"Introduction to Industrial Internet of Things and Industry 4.0" Sudip Misra, Chandana Roy, Anandarup Mukherjee 2021
2	
3	

References	
1	D.E. Comer "Internetworking with TCP/IP", Vol. I (4th Edition), II, III (PHI)
2	Olivier Hersent, David Boswarthick "Internet of Things Applications and Protocols ", Wiely publication 2nd Ed.
3	William Stallings "Foundations of Modern Networking : SDN, NFV, QoE, IoT and Cloud" Pearson Education

Useful Links	
1	https://onlinecourses.nptel.ac.in/noc21_cs17/preview
2	

CO-PO Mapping

	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1			3						3				2	
CO2			3											2
CO3	2													3
CO4														

The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High
Each CO of the course must map to at least one PO.

Assessment

The assessment is based on MSE, ISE and ESE.
MSE shall be typically on modules 1 to 3.
ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be quiz, seminar, assignments or any interactive activity etc. and is expected to map at least one higher order PO.
ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.
For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

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AY 2023-24

Course Information

Programme	B. Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech. Sem. VIII
Course Code	5EN492
Course Name	Project-II
Desired Requisites:	Project-I

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	-	**LA1**	**LA2**	**ESE**	**Total**
Tutorial	-	30	30	40	100
Practical	12 Hrs/Week				
Interaction	-	**Credits: 6**			

Course Objectives

1	Review and finalization of the approach to solve the problem relating to the assigned topic.
2	Finalizing objectives and expected outcomes of the project. Writing the technical specifications and product specifications of completed/ final project.
3	Detailed Analysis/Modelling/Simulation/Design/Problem Solving/Design of Experiments as required for the project-work.
4	Prepare a paper on project work for conference/ journal publication with suggested modifications and future of the project work.

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Choose/ Experiment with the method/ methodology finalized/ designed to solve the problem undertaken as project.	Apply
CO2	Model/ Simulate/ Design/ Design the experiments to verify the expected results/ specifications of project.	Analyze Evaluate
CO3	Develop the final product/process, testing, results, conclusions and future direction.	Create
CO4	Write and publish a paper for Conference Presentation/Publication in Journals, if possible. Prepare a Project Report in the standard format for being evaluated by the department committee.	Apply
CO5	Prepare an action plan for conducting the investigation, sharing of activities during completion of project work, including team work.	Apply

List of Experiments / Lab Activities

It is expected that in-depth study of the topic assigned in the light of the report prepared under Project-I shall be continued as Project-II. The objective of Project-II is to enable the student to extend further the investigative study taken up under Project-I, either fully theoretical/practical or involving both theoretical and practical work, under the guidance of a Supervisor from the Department alone or jointly with a Supervisor from the Industry. It is expected to provide a good training for the student(s) in R&D work and technical leadership.

Assessment: The final product shall be a result of Project-I and Project-II and should be demonstrated at the time of examination. A demonstration and oral examination on the Project-II shall be conducted at the end of the semester.

Text Books

1	Journal/ Conference papers/ Magazine Articles/ Handbooks with reference to topic selected for the project-work.
2	
3	
4	

References

1	Journal/ Conference papers/ Magazine Articles/ Handbooks with reference to topic selected for the project-work.
2	
3	
4	
Useful Links	
1	https://ieeexplore.ieee.org
2	https://www.sciencedirect.com
3	https://www.elsevier.com
4	

CO-PO Mapping														
	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3	3		3	3	3	2					2	3	3
CO2		2	3	3	3							2	3	3
CO3			3		2	2	2	2			2	2	3	3
CO4								3	3	3	3	2	2	2
CO5									3		3			
The strength of mapping is to be written as 1,2,3; Where, 1:Low, 2:Medium, 3:High Each CO of the course must map to at least one PO.														

Assessment				
There are three components of lab assessment, LA1, LA2 and Lab ESE. IMP: Lab ESE is a separate head of passing. LA1, LA2 together is treated as In-Semester Evaluation.				
Assessment	**Based on**	**Conducted by**	**Typical Schedule**	**Marks**
LA1	Lab activities, attendance, journal	Lab Course Faculty	During Week 1 to Week 6 Marks Submission at the end of Week 6	30
LA2	Lab activities, attendance, journal	Lab Course Faculty	During Week 7 to Week 12 Marks Submission at the end of Week 12	30
Lab ESE	Lab activities, attendance, journal	Lab Course Faculty	During Week 15 to Week 18 Marks Submission at the end of Week 18	40
Week 1 indicates starting week of a semester. The typical schedule of lab assessments is shown, considering a 26-week semester. The actual schedule shall be as per academic calendar. Lab activities/Lab performance shall include performing experiments, mini-project, presentations, drawings, programming and other suitable activities, as per the nature and requirement of the lab course. The experimental lab shall have typically 8-10 experiments.				

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Course Information

Programme	B.Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem. VIII
Course Code	5EN431
Course Name	Professional Elective 6 - System on Chip
Desired Requisites:	Embedded System Design, FPGA Based System Design

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
		Credits: 3			

Course Objectives

1	To understand the concepts of System on Chip Design methodology for Logic and Analog Cores.
2	To differentiate embedded system design and system on chip architectures.
3	To motivate students to learn implementation of SOC using MicroBlaze.
4	To teach students to develop IP based system design

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	**Understand** about SOC design methodology	Understand
CO2	**discuss** the functional and non-functional performance of the system early in the design process to support design decisions	Understand
CO3	**Apply** concepts of System on Chip Design methodology for Logic and Analog Cores	Apply
CO4	**Analyze** hardware/software trade-offs, algorithms, and architectures to optimize the system based on requirements and implementation constraints.	Analyze

Module	**Module Contents**	**Hours**
I	**Introduction to the System Approach** Concept of system, importance of system architectures, introduction to SIMD, SSID, MIMD and MISD architectures, concept of pipelining and parallelism. Designing microprocessor /Microcontroller based system and embedded system	5
II	**Introduction to SOC** Components of SOC, Design flow of SOC, Hardware/Software nature of SOC, Design Trade-offs, SOC Applications, Differences between Embedded systems and SOCs. System design issues in SOCs.	7
III	**Interconnection** On-chip Buses: basic architecture, topologies, arbitration and protocols, Introduction to AMBA bus, IBM's core connect bus, concept of PLB-processor local bus and on chip peripheral bus (OPB), implementing arbiters in design.	7
IV	**Processors** Concept of Soft embedded processors, Hard vs. Soft embedded processors, Study of Microblaze RISC processor, Programming steps in MicroBlaze Processor.	7
V	**IP based system design** Introduction to IP Based design, Types of IP, IP across design hierarchy, IP life cycle, Creating and using IP, Technical concerns on IP reuse, IP integration, IP evaluation on FPGA prototypes.	7
VI	**Application Studies/ Case Studies** SOC system design example with Peripherals like USB, UART, Ethernet Etc. using latest FPGA. (Xilinx/ Altera tools) Eclipse IDE development tool for a full SOC system design with embedded C/C++ applications (Xilinx / Altera tools)	7

Textbooks	
1	René Beuchat, Florian Depraz, Andrea Guerrieri, Sahand Kashani, “Fundamentals of System-on-Chip Design on Arm Cortex-M Microcontrollers”, ARM Education Media.
2	Michael J. Flynn and Wayne Luk, “Computer System Design System-on-Chip”, Wiley India Pvt. Ltd.
3	Steve Furber, “ARM System on Chip Architecture “, 2nd Edition, 2000, Addison Wesley Professional.
4	“A Hands-On Guide to Effective Embedded System Design”, XILINX
References	
1	Ricardo Reis, “Design of System on a Chip: Devices and Components”, 1st Edition, 2004, Springer
2	Jason Andrews, “Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology)”, Newnes, BK and CDROM.
3	Prakash Rashinkar, Peter Paterson and Leena Singh L, “System on Chip Verification – Methodologies and Techniques”, 2001, Kluwer Academic Publishers.
4	“Embedded Processor Hardware Design” UG940 (v 2013.2) February 7, 2014
Useful Links	
1	https://www.arm.com/resources/education
2	https://www.xilinx.com/
3	https://swayam.gov.in/nc_details/NPTEL
4	https://www.coursera.org/

CO-PO Mapping														
	Programme Outcomes (PO)												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	2													
CO2	2													
CO3		2			2									2
CO4			2										2	
1: Low, 2: Medium, 3: High														

Assessment
The assessment is based on MSE, ISE and ESE. MSE shall be typically on modules 1 to 3. ISE shall be taken throughout the semester in the form of teacher’s assessment. Mode of assessment can be quiz, seminar, assignments or any interactive activity etc. and is expected to map at least one higher order PO. ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6. For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

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AY 2023-24

Course Information	
Programme	B.Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem. VIII
Course Code	5EN437
Course Name	Professional Elective 6 - Advanced Embedded Programming
Desired Requisites:	Embedded System Design, Python programming

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
		Credits: 3			

Course Objectives	
1	To understand the recent advancements in Embedded System Design .
2	To motivate students to learn implementation of Linux based Embedded System Design.
3	To motivate students to learn implementation of solutions for Autonomous Vehicles using Intelligent Embedded System.
4	To teach students to develop AI based Embedded System Design.

Course Outcomes (CO) with Bloom's Taxonomy Level		
At the end of the course, the students will be able to,		
CO1	**understand** the need of python programming language in Embedded System Design.	Understand
CO2	**write** code / scripts to configure and use Embedded Web Server using Embedded Linux.	Apply
CO3	**design** AI based applications for Automotive using Embedded System Design.	Apply
CO4	**analyze** different object detection Embedded Automotive algorithms required by autonomous vehicles for decision making.	Analyze

Module	**Module Contents**	**Hours**
I	**Python for Embedded System Design** Benefits of Using Python, Memory Management in Embedded Systems, Disadvantages of Using Python, Hardware Options for Running Embedded Python, Software Options for Writing Embedded Python, Micro Python and Circuit Python, Setting Up Environment and Running Code.	6
II	**Embedded Web Server** Fundamentals of Web technology, Web server, Web Client, Server and client side scripting, Front End Design using HTML, CSS and Responsive web design, Configuration of web server on Embedded System Design, Handling hardware through python, Fundamentals of database.	7
III	**Embedded Web Server with Flask and Raspberry Pi** Installing FLASK and Setting RPi Web Server, Design and Implementation of web based application using Python and Raspberry Pi like controlling GPIO pins, reading status of GPIO, Integrating Sensors and Actuators in Web based Embedded System.	7
IV	**Intelligent Embedded Systems for Automotive** Applications of Embedded Systems in Automotive, Challenges and Limitations of Embedded Systems in Automotive, intelligent embedded software, AI in Embedded Systems.	7
V	**Object Detection for Electric / Autonomous Vehicles** Case study Advanced Driver Assistance Systems (ADAS) driven by AI, study of object detection, object categorization and decision making for vehicles using different algorithms and Embedded C / Embedded Linux platform.	7

VI	**Protocols for Embedded Automotive** Controller area network (CAN) protocol, Need of CAN in Automobiles, CAN Protocol Stack and its Layered Architecture, programming Example for CAN, overview of LoRa Technology in Vehicle Communication.	6

Textbooks	
1	"Programming Microcontrollers with Python" first edition, Apress, 2021.
2	Cem Unsalan; Duygun E. Barkana; H. Deniz Gurhan, "Embedded Digital Control with Microcontrollers: Implementation with C and Python", Wiley-IEEE Press, 2021.
3	Ovidiu Vermesan, Mario Diaz Nava, Björn Debaillie, "Embedded Artificial Intelligence Devices, Embedded Systems, and Industrial Applications", River Publishers, 2023.
4	"Exploring Raspberry Pi: Interfacing to the Real World with Embedded Linux", Wiley, 2016

References	
1	https://www.w3schools.com/nodejs/nodejs_raspberrypi.asp
2	Raj Ponnaluri and Priyanka Alluri, "Connected and Automated Vehicles", 2021
3	"Building Embedded Linux Systems",
4	Sumit Ranjan, Dr. S. Senthamilarasu, "Applied Deep Learning and Computer Vision for Self-Driving Cars", Packt Publishing, 14 August 2020.

Useful Links	
1	https://www.edx.org/
2	https://www.udacity.com/
3	https://www.coursera.org/
4	https://www.kernel.org/

CO-PO Mapping

	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	2													
CO2		2												
CO3			2		2									
CO4				2										2
1: Low, 2: Medium, 3: High														

Assessment

The assessment is based on MSE, ISE and ESE.

MSE shall be typically on modules 1 to 3.

ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be quiz, seminar, assignments or any interactive activity etc. and is expected to map at least one higher order PO.

ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.

For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

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AY 2023-24

Course Information	
Programme	B.Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem VIII
Course Code	5EN433
Course Name	Professional Elective 7-Radar and Navigation
Desired Requisites:	Communication Engineering

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	0 Hrs/week	30	20	50	100
		Credits: 3			

Course Objectives	
1	To learn Radar fundamentals and analysis of the radar signals.
2	To understand various technologies involved in the design of radar transmitters and receivers.
3	To learn various radars like MTI, Doppler and tracking radars and their comparison.
4	

Course Outcomes (CO) with Bloom's Taxonomy Level		
At the end of the course, the students will be able to,		
CO1	Demonstrate an understanding of the factors affecting the radar performance using Radar Range Equation	Understand
CO2	Analyze the principle of FM-CW radar	Analyze
CO3	Identify the different types of Radar Displays and their application in real time scenario	Apply
CO4	Demonstrate the importance of Matched Filter Receivers in Radars	Understand

Module	**Module Contents**	**Hours**
I	**Basics of Radar**: Introduction, Maximum Unambiguous Range, Simple form of Radar Equation, Radar Block Diagram and Operation, Radar Frequencies and Applications. Prediction of Range Performance, Minimum Detectable Signal, Receiver Noise, Modified Radar Range Equation, Illustrative Problems. **Radar Equation** : SNR, Envelope Detector — False Alarm Time and Probability, Integration of Radar Pulses, Radar Cross Section of Targets (simple targets – sphere, cone-sphere), Transmitter Power, PRF and Range Ambiguities, System Losses (qualitative treatment), Illustrative Problems.	7
II	**CW and Frequency Modulated Radar:** Doppler Effect, CW Radar — Block Diagram, Isolation between Transmitter and Receiver, Non-zero IF Receiver, Receiver Bandwidth Requirements, Applications of CW radar. Illustrative Problems **FM-CW Radar:** Range and Doppler Measurement, Block Diagram and Characteristics, FM-CW altimeter, Multiple Frequency CW Radar	7
III	**MTI and Pulse Doppler Radar:** Introduction, Principle, MTI Radar with – Power Amplifier Transmitter and Power Oscillator Transmitter, Delay Line Cancelers — Filter Characteristics, Blind Speeds, Double Cancellation, Staggered PRFs. Range Gated Doppler Filters. MTI Radar Parameters, Limitations to MTI Performance, MTI versus Pulse Doppler Radar.	6
IV	**Tracking Radar**: Tracking with Radar, Sequential Lobing, Conical Scan, Monopulse Tracking Radar — Amplitude Comparison Monopulse (one- and two- coordinates), Phase Comparison Monopulse, Tracking in Range. Acquisition and Scanning Patterns. Comparison of Trackers.	6

V	**Detection of Radar Signals in Noise** : Introduction, Matched Filter Receiver – Response Characteristics and Derivation, Correlation Function and Cross-correlation Receiver, Efficiency of Non-matched Filters, Matched Fitter with Nonwhite Noise. **Radar Receivers** – Noise Figure and Noise Temperature. Displays — types. Duplexers — Branch type and Balanced type. Circulators as Duptexers. Introduction to Phased Array Antennas – Basic Concepts, Radiation Pattern, Beam Steering and Beam Width changes, Applications. Advantages and Limitations.	6
VI	**Radar Clutter and Basic Navigational Radar System 9** Introduction to Radar Clutter - Types, Surface clutter radar equation, Fundamentals of Navigation aids: Types of Navigation aids, ILS, DME, VOR, TACAN, MLS, LORAN, DECCA, OMEGA,	7

Textbooks	
1	Skolnik, Merrill Ivan. Introduction to Radar Systems , TMH Special Indian Edition, 2nd Ed.. 2007. ISBN: 9780072881387
2	Raju, G. S. N.. Radar engineering. India, I.K. International Publishing House Pvt. Limited, 2008., ISBN: 9788190694216
3	
4	

References	
1	Mark A. Rkhards, James A. Scheer, William A. HoIm. Yesdee , Principles of Modem Radar: Basic Principles –, Scitech Publication, 2013, ISBN: 9781613532010
2	Radar Principles. India, Wiley India Pvt. Limited, 2007., ISBN: 9788126515271
3	

Useful Links	
1	https://archive.nptel.ac.in/courses/108/105/108105154/
2	

CO-PO Mapping

	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3													
CO2				3										
CO3				3										
CO4	3													

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO.

Assessment

The assessment is based on MSE, ISE and ESE.
MSE shall be typically on modules 1 to 3.
ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.
ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.
For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

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AY 2023-24

Course Information	
Programme	B.Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem VIII
Course Code	5EN434
Course Name	Professional Elective 7-Data Analytics
Desired Requisites:	Probability and Statistics

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	-	30	20	50	100
		Credits: 3			

Course Objectives	
1	Develop in depth understanding of the key technologies in data science and business analytics:
2	Use quantitative modeling and data analysis techniques to the solution of real world business problems, communicate findings, and effectively present results using data visualization techniques
3	
4	

Course Outcomes (CO) with Bloom's Taxonomy Level

At the end of the course, the students will be able to,

CO1	Describe various concepts of data analytics pipeline	Understand
CO2	Apply classification, regression, mining techniques on streaming data	Apply
CO3	Compare different clustering and frequent pattern mining algorithms	Analyze
CO4	Describe the concept of R programming and implement analytics on Big data using R	Evaluate

Module	**Module Contents**	**Hours**
I	**Introduction to Data Analytics**: Sources and nature of data, classification of data (structured, semi-structured, unstructured), characteristics of data, introduction to Big Data platform, need of data analytics, evolution of analytic scalability, analytic process and tools, analysis vs reporting, modern data analytic tools, applications of data analytics. **Data Analytics Lifecycle**: Need, key roles for successful analytic projects, various phases of data analytics lifecycle – discovery, data preparation, model planning, model building, communicating results, operationalization.	5
II	**Data Analysis** Regression modeling, multivariate analysis, Bayesian modeling, inference and Bayesian networks, support vector and kernel methods, analysis of time series: linear systems analysis & nonlinear dynamics, rule induction, neural networks: learning and generalisation, competitive learning, principal component analysis and neural networks, fuzzy logic: extracting fuzzy models from data, fuzzy decision trees, stochastic search methods.	8
III	**Mining Data Streams** Introduction to streams concepts, stream data model and architecture, stream computing, sampling data in a stream, filtering streams, counting distinct elements in a stream, estimating moments, counting oneness in a window, decaying window, Real-time Analytics Platform (RTAP) applications, Case studies – real time sentiment analysis, stock market predictions	8

IV	**Frequent Item sets and Clustering** Mining frequent itemsets, market based modelling, Apriori algorithm, handling large data sets in main memory, limited pass algorithm, counting frequent itemsets in a stream, clustering techniques: hierarchical, K-means, clustering high dimensional data, CLIQUE and ProCLUS, frequent pattern based clustering methods, clustering in non-euclidean space, clustering for streams and parallelism.	7
V	**Frame Works and Visualization** MapReduce, Hadoop, Pig, Hive, HBase, MapR, Sharding, NoSQL Databases, S3, Hadoop Distributed File Systems, Visualization: visual data analysis techniques, interaction techniques, systems and applications	7
VI	**Introduction to R** R graphical user interfaces, data import and export, attribute and data types, descriptive statistics, exploratory data analysis, visualization before analysis, analytics for unstructured data	5

Textbooks	
1	Rechard Dosey, "Data Analytics: Become A Master In Data Analytics Paperback"
2	Mark Gardner, "Beginning R: The Statistical Programming Language", Wrox Publication
3	
4	

References	
1	David Dietrich, Barry Heller, Beibei Yang, "Data Science and Big Data Analytics", EMC Education Series, John Wiley
2	Michael Berthold, David J. Hand, Intelligent Data Analysis, Springer
3	Anand Rajaraman and Jeffrey David Ullman, Mining of Massive Datasets, Cambridge University Press
4	

Useful Links	
1	
2	
3	

CO-PO Mapping

	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3													
CO2			3											
CO3		3												
CO4					3								2	

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO.

Assessment

The assessment is based on MSE, ISE and ESE.
MSE shall be typically on modules 1 to 3.
ISE shall be taken throughout the semester in the form of teacher's assessment. Mode of assessment can be field visit, assignments etc. and is expected to map at least one higher order PO.
ESE shall be on all modules with around 40% weightage on modules 1 to 3 and 60% weightage on modules 4 to 6.
For passing a theory course, Min. 40% marks in (MSE+ISE+ESE) are needed and Min. 40% marks in ESE are needed. (ESE shall be a separate head of passing)

Walchand College of Engineering, Sangli *(Government Aided Autonomous Institute)*					
AY 2023-24					
Course Information					
Programme	B.Tech. (Electronics Engineering)				
Class, Semester	Final Year B. Tech., Sem VIII				
Course Code	5EN432				
Course Name	Professional Elective 8 -Digital System Engineering				
Desired Requisites:	Digital Design				
Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	- Hrs/week	30	20	50	100
		Credits: 3			

Course Objectives	
1	To understand the fundamental issues such as power, noise, signaling and timing associated with high speed digital systems.
2	To analyze the effect of parasitic of wires/interconnects in restricting the high speed performance of digital circuits and design the approaches to tackle this associate problem by using their engineering models
3	To comprehend the different sources of interference (noise) in digital systems and apply engineering/statistical models of these to compute and compare bit error rates
4	Understand the significance of signaling & timing issues and apply the knowledge of encoding a signal for error-free transfer of information (bits) from one location to another

Course Outcomes (CO) with Bloom's Taxonomy Level		
At the end of the course, the students will be able to,		
CO1	Understand Interconnects as design objects, Noise in digital systems and its impact to system operation	Understand
CO2	Analyze Timing and synchronization for functional operations and signalling	Analyze
CO3	Distinguish Power distribution schemes for low noise	Apply
CO4	Explain Signal and signalling conventions for on-chip and off-chip communication	Understand

Module	Module Contents	Hours
I	**Wires:** Geometry and Electrical properties, Electrical models of wires (Ideal wire, Transmission line), Simple transmission lines (RC, lossless LC, lossy LRC transmission lines, Dielectric absorption), Special transmission lines (Multi drop buses, Balanced Transmission lines, Common and differential mode impedance, Isolated lines)	7
II	**Noise in Digital System:** Noise sources in a digital system, Power Supply Noise, Cross-talk, Inter-symbol Interference, Noise due to other sources (Alpha particles, Electro-magnetic Interference, Process variation, Thermal Noise, Shot Noise, Flicker or 1/f Noise), Managing noise.	7

III	**Signaling Conventions:** CMOS and Low swing current mode signaling system, Considerations in transmission system design, Signaling modes for transmission lines, Transmitter signaling methods, Receiver signal detection, Source termination, Under-terminated Drivers, Differential Signaling, Signaling over capacitive transmission medium, Signal encoding	7
IV	**Timing Convention:** Conventional Synchronous system and closed loop pipelined system, considerations in timing design, Timing fundamentals, Timing properties of combinational logic and clock storage elements, Eye diagram, Encoding Timing (Signals and Events), Open loop synchronous timing, Closed loop timing, Phase locked loops, Clock Distribution	6
V	**Synchronization:** Synchronization Fundamentals, Applications of synchronization (Arbitration of asynchronous signals, Sampling asynchronous signals, Crossing clock domains), Synchronization failure and meta-stability, Synchronizer Design (Mesochronous, Plesiochronous, Periodic Asynchronous)	6
VI	**Power Distribution:** The power supply network (Local loads, Signal loads), Local Regulation, Logic loads and on-chip power supply distribution (Logic current profile, IR drops, Area Bonding, On-chip by-pass capacitor), Power supply isolation (Supply-supply isolation, Signal-supply isolation), Bypass capacitors, Power Distribution system	6

Textbooks	
1	*Digital System Engineering,* William Dally and John Poulton, Cambridge University Press, Reprint 2007
2	

References	
1	*High Speed Digital Design, A Handbook of Black Magic,* Howard W. Johnson, Martin Graham, Prentice Hall PTR, Englewood Cliffs, NJ 0763.
2	*High Speed Digital System Design: Interconnect Theory and Design Practices"* Stephen H. Hall, Garrett W. Hall, James A. McCall, Wiley-IEEE Press (ISBN: 978-0-471-36090-2

Useful Links	
1	http://cva.stanford.edu/books/dig_sys_engr/
2	
3	

CO-PO Mapping

	Programme Outcomes (PO)												**PSO**	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
CO1	3													
CO2	3													
CO3				3										
CO4				3										

The strength of mapping is to be written as 1: Low, 2: Medium, 3: High
Each CO of the course must map to at least one PO.

Assessment
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Walchand College of Engineering, Sangli

(Government Aided Autonomous Institute)

AY 2023-24

Course Information	
Programme	B.Tech. (Electronics Engineering)
Class, Semester	Final Year B. Tech., Sem VIII
Course Code	5EN435
Course Name	Professional Elective 8-Satellite Communication
Desired Requisites:	Communication Engineering

Teaching Scheme		**Examination Scheme (Marks)**			
Lecture	3 Hrs/week	**MSE**	**ISE**	**ESE**	**Total**
Tutorial	0 Hrs/week	30	20	50	100
		Credits: 3			

Course Objectives	
1	To prepare students to excel in basic knowledge of satellite communication principles
2	To provide students with solid foundation in orbital mechanics and launches for the satellite communication.
3	To train the students with a basic knowledge of link design of satellite with a design examples
4	To provide better understanding of multiple access systems and earth station technology and prepare students with knowledge in satellite navigation and GPS & and satellite packet communications

Course Outcomes (CO) with Bloom's Taxonomy Level		
At the end of the course, the students will be able to,		
CO1	Understand satellite orbit mechanics and subsystem components	Understand
CO2	Analyze the earth segment and space segment with multiple access technology	Analyze
CO3	Design various satellite link for various applications	Apply
CO4		

Module	**Module Contents**	**Hours**
I	**Communication Satellite:** Orbit and Description: A Brief history of satellite Communication, Satellite Frequency Bands, Satellite Systems, Applications, Orbital Period and Velocity, effects of Orbital Inclination, Azimuth and Elevation, Coverage angle and slant Range, Eclipse, Orbital Perturbations, Placement of a Satellite in a Geo-Stationary orbit	7
II	**Satellite Sub-Systems:** Attitude and Orbit Control system, TT &C subsystem, Attitude Control subsystem, Power systems, Communication subsystems, Satellite Antenna Equipment. **Satellite Link**: Basic Transmission Theory, System Noise Temperature and G/T ratio, Basic Link Analysis, Interference Analysis, Design of satellite Links for a specified C/N, (With and without frequency Re-use), Link Budget	7
III	**Propagation effects:** Introduction, Atmospheric Absorption, Cloud Attenuation, Tropospheric and lonospeheric Scintillation and Low angle fading, Rain induced attenuation, rain induced cross polarization interference	6
IV	**Multiple Access:** Frequency DivisIon Multiple Access (FDMA) – Intermodujation Calculation of C/N, Time Division Multiple Access (TDMA) – Frame Structure, Burst Structure, Satellite Switched TDMA, On-board Processing, Demand Assignment Multiple Access (DAMA) — Types of Demand Assignment, Characteristics, CDMA Spread Spectrum Transmission and Reception	7
V	**Earth Station Technology:** Transmitters, Receivers, Antennas, Tracking Systems, Terrestrial Interface, Power Test Methods, Lower Orbit Considerations	6

VI	**Satellite Navigation and GPS System**s: Radio and Satellite Navigation, GPS Position Location Principles, GPS Receivers, GPS C/A Code Accuracy, Differential GPS.	6

Textbooks	
1	Satellite Communications Dennjs Roddy, 2nd Edition, 1996, McGraw Hill.
2	Satellite Communications —Timothy Pratt, Charles Bostian, Jeremy Allnutt, 2nd Edition, 2003, John Wiley & Sons
3	
4	
References	
1	Satellite Communications: Design Principles — M. Richcharia, 2nd Ed., BSP, 2003.
2	Fundamentals of Satellite Communications — K. N. Raja Rao, PHI, 2004.
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Useful Links	
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	Programme Outcomes (PO)												PSO	
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